MODELING THE TEMPERATURE DEPENDENCE OF THE SILICON-ON-INSULATOR MOSFET FOR HIGH-TEMPERATURE APPLICATIONS

BY

DEOK-SU JEON

A DISSERTATION PRESENTED TO THE GRADUATE SCHOOL
OF THE UNIVERSITY OF FLORIDA IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

UNIVERSITY OF FLORIDA

1990

ACKNOWLEDGEMENTS

I wish to express a very deep sense of gratitude to my advisor, Professor Dorothea E. Burk, for her support and guidance throughout the course of this work. I would also like to thank the other members of my committee, Professors Jerry G. Fossum, Sheng S. Li, Robert M. Fox, and Kevin S. Jones, for their participation on my supervisory committee.

I am grateful to the Florida High Technology and Industry Council for the financial support that made this work possible. I wish to acknowledge Dr. Wade A. Krull and Harris Semiconductor for providing test devices. Thanks are also extended to many of my friends, Han-Jin Cho, Jin-Young Choi, Young-Sun Eo, Ho-Cheol Jang, and Sang-Gug Lee for helpful discussions and encouragement.

Last, I wish to express my gratitude to my wife and children, my parents, my parents-in-law, and my brothers and sisters for their love, patience, encouragement, and support.

TABLE OF CONTENTS

Abstract of Dissertation Presented to the Graduate School of the University of Florida in Partial Fulfillment of the Requirements for the Degree of Doctor of Philosophy

MODELING THE TEMPERATURE DEPENDENCE OF THE SILICON-ON-INSULATOR MOSFET FOR HIGH-TEMPERATURE APPLICATIONS

By

DEOK-SU JEON

December, 1990

Chairman: Dr. D. E. Burk
Major Department: Electrical Engineering

This dissertation concerns the physical modeling of temperature-dependent parameters in silicon-on-insulator (SOI) MOSFET device characteristics for high-temperature applications. A new model for the SOI MOSFET that accounts for the temperature dependences has been developed. The temperature dependences include the variation in threshold voltage which depends on the back-gate bias and body-film thickness, the increase of leakage current with temperature, the channel mobility degradation at high temperature, and the reduction in the kink effect in the output current-voltage characteristics at high temperature. A new temperature-dependent model for electron channel mobility is also developed, which accounts for dependences of electron channel mobility limited by three dominant scattering

mechanisms for the carrier transport in the MOSFET channel on temperature and on vertical electric field.

The developed models have been implemented in the circuit simulator SPICE2. The effectiveness for circuit simulation and the predictive capability of the models are demonstrated through simulations of devices and circuits at various temperatures and comparisons with measurements. The simulation of high-temperature operation of a simple smart-power integrated circuit which uses SOI CMOS as gate drive circuits is also successfully performed. The simulation is accomplished using SPICE2 extended to include the models developed and an existing power-MOSFET model. The temperature dependences of the device parameters for the power-MOSFET model are also presented.

CHAPTER 1
INTRODUCTION

Silicon device technology is now being employed to interface computers to the physical world through sensors and actuators. Much of the motivation for this derives from the ability of silicon devices to merge signal processing circuitry on the same chip with the transducer. This on-chip electronics is increasingly important as sensors are being applied in such area as automobile and jet engine control, deep-well instrumentation, and nuclear power plant diagnostics and safety monitoring [Bro87]. The integration of appropriate electronics for these applications is limited by the maximum operating temperature of the circuitry, which may be well below that of the target environment. The range of applications of solid-state sensors with signal processing circuitry could be expanded if the circuit could operate reliably at elevated temperatures. The use of junction-isolated bulk CMOS at high temperature ($T \geq 250^{\circ}C$) is limited by large leakage current at the junctions and by latchup which is triggered by junction leakage current. Epi-CMOS, which uses epi-layer to improve latchup susceptibility by reducing lateral resistance, does not allow for much of an increase in the operating temperature [Bro89].

Silicon-on-insulator (SOI) technology is a promising alternative to bulk CMOS, although it still represents a significantly more expensive process. The near perfect isolation between devices in SOI as seen in Fig. 1.1 eliminates latchup, while allowing higher packing density. Because there are no large junction areas in this technology, the leakage current is much lower. The functionality of SOI CMOS circuits at T = 300°C which is much higher than that for bulk CMOS or epi-CMOS has already been observed [Kru88].

The current-voltage characteristics for the SOI MOSFET depend on two major differences which do not exist in the bulk MOSFET. The first of these is the effect of the back-gate (substrate) bias V_{GbS} on the conduction of the inversion region at the interface between the front gate oxide and the silicon body film (will be called as "front surface") [Lim85, Vee88]. The threshold voltage at the front surface V_{Tf} varys linearly with the body voltage V_{BS}, or the back gate bias V_{GbS}, depending on the magnitude of V_{GbS} [Lim83]. The second difference is the effect of the body-film which is left as floating to eliminate the extra surface area needed for the contact to the thin-film body. Holes (in n-channel device) generated by impact ionization in the drain region are attracted into the floating body, raising the potential of the accumulation region at the back interface. This causes an increase in the drain current of the SOI

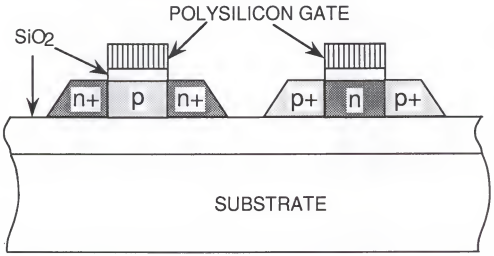


Fig. 1.1 A typical Silicon-on-insulator (SOI) CMOS structure.

MOSFET through the decrease of V_{Tf}, resulting in a kink in the I_D-V_{DS} characteristics.

These two differences effect the device characteristics of the SOI MOSFET at high temperatures. High-temperature MOSFET operation depends on the temperature dependences of several device parameters. The increase of intrinsic carrier density with increasing temperature causes the threshold voltage of the front channel to decrease, because of the decrease of the Fermi potential in the neutral body with increasing intrinsic carrier density. The threshold voltage becomes very small at high temperature, so for proper high-temperature device operation this reduction in V_{Tf} must be considered in the device design. Because the intrinsic carrier density increases with increasing temperature, the relatively low-doped thin-film body of SOI MOSFET can be intrinsic at some high temperature. To prevent this unwanted situation, the body doping concentration must be carefully chosen. The variation of threshold voltage with temperature of the thin-film SOI MOSFET can be smaller than that of bulk MOSFET. (The difference in rate of variation of V_{Tf} is due to the different rate of variation of electric field at the front surface edge of the depletion region, E_{sf}, which depends on back gate bias condition and body film thickness. The thin-film-depleted (TFD) mode of thin-film SOI MOSFET [Lim83], where the back surface is depleted during the strong inversion at the front surface, can result in a smaller variation of V_{Tf} with temperature if the back gate bias is

chosen so that the electric potential at the back surface is much larger than zero.)

At higher temperatures, the leakage current at the reverse biased body-drain junction and the depleted body film becomes larger with increasing thermal generation. Because the body-drain junction area of SOI MOSFET is smaller than that of bulk device, the leakage current may be much smaller than bulk device. However, this effect can be offset by a smaller generation lifetime due to a larger defect density in SOI.

At high temperatures, the phonon scattering is a dominant scattering mechanism for channel mobility [Sun80]. Therefore the channel mobility can be approximately represented by the phonon-scattering-limited-mobility. The degradation of channel mobility at high temperature due to the increased scattering results in the reduction of drain current, hence, the increase in switching delay.

The reduction in drain current, the increase of drain saturation voltage due to threshold-voltage reduction and the increased scattering at high temperatures cause the kink in I_D-V_{DS} characteristics of SOI MOSFET having a floating body to occur at larger drain bias, which can be advantageous.

There are some previous studies on the temperature-dependent operation of the bulk MOSFET [Sho84, Hos85] and on the room-temperature operation of the SOI MOSFET [Lim85, Vee88]. However, there exists no model for the SOI MOSFET that accounts for high-temperature effects. This dissertation, then, is concerned with temperature dependences

of the SOI MOSFET for high-temperature applications. It will facilitate an understanding of the device characteristics of the SOI MOSFET at high temperatures, the design of SOI circuits for high-temperature applications, and the ways to improve the device performance by informed device design. The main contributions made in the work are:

(1) the development of physical models for the high-temperature operation of the SOI MOSFET;

(2) the development of a physically based temperature-dependent channel mobility model;

(3) the implementation of these models into the circuit simulator SPICE2 [Nag75]; and

(4) the simulation of a simple smart-power IC using SOI CMOS in the control circuitry.

In Chapter 2, a physically based temperature-dependent channel mobility model is presented. This model accounts for the dependence of the three dominant scattering mechanisms for the carrier transport in the MOSFET channel on temperature and on vertical electric field.

In Chapter 3, the temperature dependences of the SOI MOSFET device parameters are investigated. One of these is the variation of threshold voltage with temperature as a function of the variation in Fermi potential of body-film. The V_{Tf} reduction with increasing temperature, which depends on the back-gate bias, the body-film thickness and the body doping concentration, is considered. The leakage current mechanisms at the reverse-biased body drain junction and the

depleted film are investigated. The physical models are implemented into the circuit simulator SPICE2 which contains the room-temperature thin-film SOI MOSFET model [Vee88].

In Chapter 4, the upgraded SPICE2 circuit simulator, which includes temperature-dependent models presented in Chapter 3, is used to simulate a simple smart-power IC at 300°C. The simulation of the power-MOSFET (vertical DMOST) switch at 300°C utilizes a temperature-dependent subcircuit model. Simulations of an SOI CMOS inverter and a 5-stage SOI CMOS ring oscillator are done to demonstrate the ability of the physical model proposed in Chapter 3 and the difference of the high-temperature performance of SOI CMOS circiuts from those at room temperature.

In Chapter 5 the main accomplishments of this dissertation are summarized and suggestions of areas for future work are made.

In Appendix A, the derivation of the regions where the thermal generation rate is maximized in the reverse biased p-n junction and in the depleted body film is presented.

In Appendix B, the implementation of channel mobility model into the existing drain current model of the SOI MOSFET [Vee88] is explained. Unlike the other models presented in Chapter 3, the channel mobility model cannot be directly implemented into the existing circuit model.

CHAPTER 2
CHANNEL MOBILITY MODEL

2.1 Introduction

The range of applications for MOSFET's has been expanded to include operating temperatures other than room temperature in order to exploit certain advantages for device operations [Gae77, Sch84, Gil85, Han86, Kru88]. Because of scaled-down dimensions, the inclusion of high field effects is required in understanding of the device characteristics of MOSFETs. To perform successful circuit or device simulations, a model for channel mobilities with accurate functional dependencies on temperature and on electric field is essential. A purely physical model which doesn't require the extraction of empirical parameters is most desirable. However, the channel mobility as well as the bulk mobility can be complex functions of the different scattering mechanisms and a purely physical model might be too complicated for circuit and device simulations.

The physical modeling of channel mobility is complicated further by the formation of energy subbands in the dimension perpendicular to the channel [Lin88]. A detailed explanation of the carrier distribution in these subbands and subband energies and cross-sections as a function of temperature and transverse electric field has been given recently by M. S.

Lin [Lin88]. He shows by calculations based on the work of F. Stern [Ste72] that at low temperatures ($T \leq 77$ K) the majority of carriers in the channel are in the lowest subband. This subband has the smallest cross-section perpendicular to the channel and, thus, the carriers are more tightly confined at the silicon/silicon dioxide interface. Their tight confinement results in mobility degradation caused by oxide-charge scattering at low transverse fields and surface roughness scattering at high fields. At around room temperature ($T \cong 300$ K) and low fields the carrier mobility is less affected by surface-roughness scattering as more carriers are in the higher, wider subbands and phonon scattering dominates. However, at high fields (8×10^5 V/cm), the subbands are separated further in energy and there are more carriers in the lowest, shallower subband, so surface-roughness scattering becomes important.

Because of these complications, a physically based semi-empirical model for channel mobility is needed for circuit and device simulation. The empirical parameters in the model should be minimal in number and simple to extract. The model should depend on the two independent operating conditions, temperature and transverse electric field, and possibly other design parameters such as dopant concentration, oxide-charge density, and surface roughness. Such models have been proposed by Arora et al. [Aro87] and Lombardi et al. [Lom88]. The model by Arora et al. is valid for low to high transverse fields having inversion carrier concentrations of 10^{12} cm^{-2} to

10^{13} cm^{-2} and for temperatures 77 K < T < 400K. The model by Lombardi et al. is a general model which simplifies to the bulk mobility when no channel is present and it includes the effect of both the transverse and longitudinal electric fields in the channel. It is valid over the same transverse fields, but for temperatures 200 K < T < 400 K. These two models [Aro87, Lom88] for channel mobilities are achieved by employing the Mathiessen approach; they are the addition of the reciprocal mobilities for phonon, oxide-charge and surface-roughness scattering. These models depend explicitly on dopant concentration and oxide-charge density and implicitly on surface roughness and they both have four or five empirical parameters which must be extracted.

We propose a semi-empirical model for channel mobilities in the MOSFET inversion layer at low longitudinal (drain) electric fields which contains the same scattering mechanisms, but is more physically based than the above two models. The functional dependencies of the different scattering mechanisms on the temperature and transverse electric field are more accurate and less empirical than dependencies of the corresponding mechanisms in the above models. The experimental determination of channel mobility data for 77 K < T < 370 K and parameter extraction procedure will be discussed. The proposed model is demonstrated to adequately simulate the data. The implicit dependencies of the extracted parameters on oxide charge density and surface roughness at the $Si-SiO_2$ interface have the expected trends.

The differences in the scattering mechanisms incorporated into the proposed model and the model of Arora et al. are exemplified by the resulting simulations of the experimental data.

2.2. The Model

A literature search has been conducted to identify the transverse field and temperature dependence for different scattering mechanisms which influence channel mobility. The model which we propose assumes that the channel mobility is the reciprocal sum of mobilities derived from these different scattering mechanisms. The three dominant scattering mechanisms are Coulomb, phonon, and surface-roughness scattering [Sah72, Sun80b, And82]. Thus,

$$\frac{1}{\mu} = \frac{1}{\mu_c} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}} \tag{2.1}$$

where μ is the channel mobility, and μ_c, μ_{ph}, and μ_{sr} are the mobilities derived from Coulomb, phonon, and surface roughness scattering, respectively.

The relative importance of these different scattering mechanisms from 4.2 K < T < 300 K is clearly defined in the data of Hall mobility as a function of inversion carrier concentration for two samples having oxide charge density 8 x 10^{10} cm^{-2} and 7.4 x 10^{10} cm^{-2} given in Fig. 47 of [And82]. To clarify the discussion, a schematic of this figure is given in Fig. 2.1. The channel mobility at 300 K is smaller than

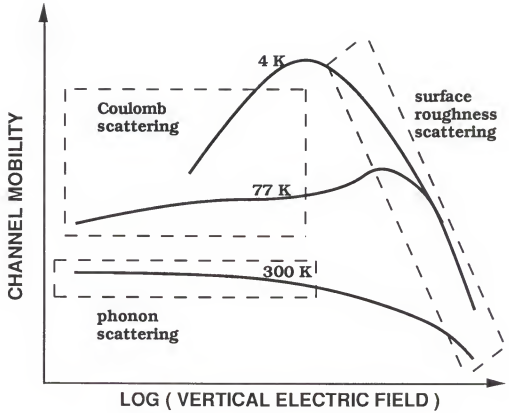


Fig. 2.1 A schematic for the dependence of channel mobility on vertical electric field, as a function of temperature. The regions where a specific scattering mechanism is dominant are indicated in the boxes.

that at low temperatures and less dependent on the roughness of surface or oxide charge density. At these temperatures, phonon scattering dominates at low and intermediate fields. The channel mobility is much more dependent on oxide charge and inversion layer carrier concentration at low temperatures and peaks at intermediate transverse fields. At low inversion layer carrier concentrations, the mobility increases as oxide charge scattering decreases because of carrier screening. At carrier concentrations above the peak, the mobility decreases as surface roughness scattering predominates. The magnitude of the mobility at the peak is very sensitive to oxide charge density and temperature at the low end of this temperature range and decreases in magnitude and sensitivity as the temperature approaches 77 K. The mobility is very temperature dependent at low inversion layer carrier concentration and temperature-independent at high surface inversion carrier concentrations.

2.2.1 Coulomb-Scattering-limited Mobility

The temperature dependencies of Coulomb scattering are different between the room temperature and the 77 K cases [And82]. Coulomb-scattering-limited mobility is modeled separately in the high temperature range (100 K < T < 370 K) and the low temperature range (77 K < T < 100 K).

2.2.1.1 High Temperature Range

The effect of Coulomb scattering at high temperatures is small, since the carriers are moving faster and are therefore scattered less by the Coulomb scatterers. However, it can't be neglected because oxide charge contributes to the scattering even at room temperature [Sah72, Sun80b].

Sah et. al. [Sah72] has formulated the scattering of electrons by surface oxide charges and by ionized impurities by treating the random spatial fluctuations of charge density as a perturbation. The theory is applied to a simple two-dimensional model with a random Poisson distribution of oxide charges, giving the Coulomb-scattering-limited mobility

$$\mu \propto \frac{T}{N_I} \tag{2.2}$$

where T is a temperature and N_I is the interface charge density at the $Si-SiO_2$ interface. Following this result we model μ_c in the high temperature as

$$\mu_c = \frac{T}{a_c} \tag{2.3}$$

where a_c is a parameter to be extracted.

2.2.1.2 Low Temperature Range

The temperature dependence of μ_c at the low temperatures is different from that at the high temperatures. The discrepancy could be due to the fact that the screening effect is appreciable at low temperatures. The increase in

the kinetic energy of electrons with increasing temperature tends to reduce the scattering and at the same time reduces the screening effect. Therefore the actual temperature dependence is determined by the relative importance of these two effects.

Stern [Ste78] has found that the decrease in carrier screening is much more important and it reduces the mobility limited by Coulomb scattering. He [Ste80] calculates the Coulomb scattering rate in the inversion layer using the full dependence of the screening parameter q_s on temperature T and on wave-vector q_w. He finds the Coulomb scattering rate increases approximately linearly with temperature from zero to about 40 K. He also finds the scattering rate is related to the inversion layer carrier concentration N_s and it is proportional to $N_s^{1.9\pm0.1}$ for a sample. These results are supported by experiments of Cham and Wheeler[Cha80].

Kawaguchi et. al. [Kaw80] has measured the dependence of mobility on the carrier concentration N_s at temperatures T = 1.5 - 70 K for high- and low-mobility MOSFETs. The low-mobility samples have relatively large numbers of interface charge (Coulomb scatterer) at the semiconductor-insulator interface, while the high-mobility samples have fewer Coulomb scatterers. They find from measurement that the Coulomb scattering rate depends on N_s such that $\mu_c^{-1} \propto N_s^{1.9}$ in low mobility samples which is in agreement with Stern's theory. In high-mobility samples, the rate is proportional to $N_s^{1.6}$ in low N_s region.

Therefore, the Coulomb scattering mobility μ_c for the low-temperature model is

$$\mu_c \propto \frac{N_s^{\alpha}}{T} \tag{2.4}$$

where α=1.6 - 2 depending on oxide charge density but it should be a constant for the devices from the same process.

The effective electric field in the inversion layer E_{eff} is to be [Sun80b, Sab79, Mat74]

$$E_{eff} = \frac{q\left(\frac{N_s}{2} + N_{dep}\right)}{\varepsilon_s} \tag{2.5}$$

where q is the electron charge and ε_s is the permittivity of silicon and N_{dep} is the depletion region charge density. So assuming $N_s >> N_{dep}$ at strong inversion,

$$E_{eff} \propto N_s \tag{2.6}$$

The Coulomb scattering limited mobility at low temperatures is modeled as

$$\mu_c = \frac{E_{eff}^{\alpha}}{a_c\, T} \tag{2.7}$$

where a_c is a parameter to be extracted.

2.2.2 Phonon-scattering-limited mobility

2.2.2.1 Low Temperature Range

Assuming that all the inversion layer electrons are in the lowest subband (the electric quantum limit), Kawaji [Kaw69] modeled the mobility limited by acoustic phonon scattering in the inversion layer at room temperature as,

$$\mu_{ac} \propto \frac{1}{T\ N_s^{1/3}} \tag{2.8}$$

However, this result is not generally valid at room temperature, where the carriers can undergo intervalley and intersubband phonon scattering [Eza74]. Sah et al. [Sah72] found that Kawaji's result is valid for T < 100 K where only surface acoustical phonons are important for the phonon scattering. Therefore, the mobility limited by acoustic phonon scattering at T < 100 K from (2.8) and (2.6) is

$$\mu_{ph} = \frac{1}{a_p\ T\ E_{eff}^{1/3}} \tag{2.9}$$

where a_p is a parameter to be extracted.

2.2.2.2 High Temperature Range

For intermediate inversion layer concentrations(N_s = 0.5 - 5 x 10^{12} cm^{-2}) at room temperature, the channel mobility has been observed to have dependence on N_s and T [Eza74],

$$\mu_{ph} \propto \frac{1}{T^n\ N_s^{1/\gamma}} \tag{2.10}$$

where γ = 3 - 6 and n = 1 - 1.5. The γ and n depend on crystallographic orientation of the surface chosen, but are independent of the device fabrication processes. So for devices with same orientation of the surface, n and γ can be fixed in the magnitude. If the carriers lie in the fundamental subband and undergo intrasubband scattering only, n = 1 and γ = 3 [Kaw69, Eza74] as in (2.8). The intervalley and intersubband scatterings cause n to increase, while the intersubband scattering tends to increase γ. The magnitude of the calculated μ_{ph} in the range of N_s = 0.5 - 5 x 10^{12} cm^{-2} is much larger than that of measured mobility at that range of N_s [Eza74]. Stern [Ste80] found that mobility limited by Coulomb scattering should be included in that range of N_s. According to Ando et al. [And82] the best comparison of the measured mobility at the room temperature with phonon scattering theory could be made at the range of N_s = 2 - 5 x 10^{12} cm^{-2}.

For T > 100 K, the model for phonon scattering limited mobility μ_{ph} taken from (2.10) and (2.6) is

$$\mu_{ph} = \frac{1}{a_p \, T^n \, E_{eff}^{1/\gamma}} \qquad (2.11)$$

where n and γ and initial estimate of a_p are extracted at room temperature and 2 x 10^{12} < N_s < 5 x 10^{12} cm^{-2}.

2.2.3. Surface-Roughness-Scattering-limited Mobility

Surface asperities at the $Si-SiO_2$ constitute a major cause of scattering at high electron concentrations. The dependence of the surface roughness scattering limited mobility μ_{sr} on N_s and N_{dep} [Har76, And77, Fer79, Mor79]is given by

$$\mu_{sr} \propto \frac{1}{(N_s + N_{dep})^2} \qquad (2.12)$$

The surface roughness scattering is independent of temperature [Har80]. Surface roughness scattering is dominant at high electric fields where $N_s >> N_{dep}$. So by using (2.12) and (2.6) the surface roughness scattering limited mobility is modeled

$$\mu_{sr} = \frac{1}{a_s E_{eff}^2} \qquad (2.13)$$

where a_s is a parameter to be extracted.

2.2.4 Proposed Model

For the high temperature range (100 K < T < 370 K), the total channel mobility model at low longitudinal (drain) electric field from (2.3), (2.11), and (2.13) is

$$\mu_{eff} = \frac{1}{\left(\frac{a_c}{T} + a_p T^n E_{eff}^{1/\gamma} + a_s E_{eff}^2\right)} \qquad (2.14)$$

where a_c, a_p, a_s, n, and γ are the parameters to be extracted.

For the low temperature range (77 K < T <100 K), the total mobility model which is consisted of (2.7), (2.9), and (2.13) is

$$\mu_{eff} = \frac{1}{\left(\frac{a_c T}{E_{eff}^{\alpha}} + a_p T E_{eff}^{1/3} + a_s E_{eff}^{2}\right)} \qquad (2.15)$$

where a_c, a_p, a_s, and α are the parameters to be extracted. The cutoff temperature T = 100 K between the low and high temperature range is consistent with the models for Coulomb and phonon scattering.

2.3 The Experiments

The devices are from a standard bulk NMOS process and have been fabricated on p-epi with junction isolated. They have a gate oxide thickness t_{ox} = 25 nm with an oxide charge density, a channel length L = 25 μm, and a width W = 50 μm. The gate electrode is n+ polysilicon and each device has a body as well as a substrate contact.

The temperature-dependent measurement is conducted with an automated system consisting of an HP 9000 series 217 desk top computer and HP 4145 device parameter analyzer and a Delta Design temperature-controlled environment. The effective channel mobilities and the threshold voltages are determined using TECAP [Hew86], a device parameter extraction program from Hewlett-Packard, with measurements of drain current I_D taken at small drain voltage V_{DS} as a function of

the gate bias with the source and body grounded. The resistance external to effective channel region R_{ext} and lateral diffusion of the drain and source ΔL is extracted from the measured data following the method in the ref. [Lau84]. The Levenberg-Marquart algorithm [Pre86] for the nonlinear fitting routines is used for the extraction of model parameters.

In the linear region of the MOSFET characteristic at small $V_{DS}(<<\phi_b)$ [Sze81],

$$I_D = \frac{W}{L}\,\mu_{eff}\,C_{ox}\left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right)V_{DS} \qquad I_D = \frac{W}{L}\,\mu_{eff}\,C_{ox}\left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right)V_{DS} \tag{2.16}$$

where $\phi_b = kT/q*\ln(N_{sub}/n_i)$, $C_{ox} = \varepsilon_{ox}/t_{ox}$. When the effect of the external resistance R_{ext} and lateral diffusion ΔL is considered , then

$$V_{DS} = V_{DS,ext} - R_{ext}\,I_D \tag{2.17}$$

$$V_{GS} = V_{GS,ext} - \frac{1}{2}\,R_{ext}\,I_D \tag{2.18}$$

$$L_{eff} = L - \Delta L \quad . \tag{2.19}$$

where L_{eff} is the effective channel length and L is channel length on the mask [Lau84]. Substituting (2.17), (2.18), and (2.19) into (2.16), we get

$$I_D = \frac{\frac{W}{(L - \Delta L)} \mu_{eff} C_{ox} \left(V_{GS,ext} - V_{TH} - \frac{V_{DS,ext}}{2}\right) V_{DS,ext}}{1 + \frac{W}{(L - \Delta L)} \mu_{eff} C_{ox} R_{ext} \left(V_{GS,ext} - V_{TH} - \frac{V_{DS,ext}}{2}\right)} \quad (2.20)$$

From (2.20), the effective mobility is derived as

$$\mu_{eff} = \frac{I_D}{\frac{W}{(L - \Delta L)} C_{ox} \left(V_{GS,ext} - V_{TH} - \frac{V_{DS,ext}}{2}\right) \left(V_{DS,ext} - R_{ext} - \frac{V_{DS}}{2}\right)} \quad (2.21)$$

With the measured I_D, extracted R_{ext} and ΔL, we can calculate the effective mobility from (2.21). The gate voltage at which the value of I_D in (2.16) is zero is found by extrapolating the tangent at the point of the inflection in the I_D-V_{DS} curve to zero current. The threshold voltage V_{TH} is determined by subtracting $V_{DS}/2$ from the gate voltage. The inversion layer carrier concentration N_s is found from the product of gate oxide capacitance C_{ox} and $(V_{GS} - V_{TH})$ and the effective electric field in the inversion layer E_{eff} is calculated from (2.5).

2.4 The Parameter Extraction

During the parameter extraction, specific ranges in temperature and transverse electric field are defined where phonon and surface roughness scattering dominate. First, the parameters for phonon scattering in the high temperature range (in (2.11)) are extracted from the experimental mobility data determined as described in the previous section. The powers n and $1/\gamma$ and an initial estimate for a_2 are determined by curve fitting to the room temperature data taken at intermediate transverse electric fields (2×10^{12} $cm^{-2} < N_s < 5 \times 10^{12}$ cm^{-2}). This temperature is chosen to be in agreement with the assumptions by Ezawa et al. [Eza74] from which the phonon scattering model in the high temperature range is taken. The powers n and $1/\gamma$ will be fixed at these extracted values for the remainder of the extraction process in the high temperature range, but the value for a_p will be further optimized along with a_c (in (2.3) or (2.7)) and a_s (in (2.13)). The initial estimate of a_s for surface roughness scattering is determined from fits to the experimental mobility data at the lowest temperature (77 K) and at high transverse electric field ($N_s > 5 \times 10^{12}$ cm^{-2}). If the measured data at T < 77 K is not available, the initial estimate of a_s can be derived from the measured data in Fig. 4 of Hartstein et al. [Har80]. Next, all three parameters a_c, a_p, and a_s are optimized by fitting the experimental data first in the high temperature range (T > 100 K) and then in the low temperature range (77 K < T < 100 K). In addition, in the low temperature range, one more parameter α is

extracted with initial estimate of 1.9 [Ste80]. The initial estimate for all of these parameters is important for obtaining the most physically meaningful fits to the data. This will be discussed further in the next section.

The best fit between the experimental mobility and the calculated mobility is obtained by minimizing the quantity given by

$$\sum_{k} \left(\frac{\left(\mu^{(k)}(P) - \mu^{*(k)} \right)}{\mu^{*(k)}} \right)^2$$

with respect to the vector of parameters P to be optimized. The $\mu^{(k)}(P)$ is the mobility calculated by the model ((2.1), (2.3), (2.7), (2.9), (2.11), and (2.13)) and $\mu^{*(k)}$ is the experimental mobility at the k-th data point. The nonlinear least squares fit for the optimization of the model parameters is performed using the Levenberg-Marquardt method [Pre86].

2.5 Results and Discussion

In Fig. 2.2, the simulated electron channel mobilities for the proposed physically based model are given together with the data for 77 K < T < 370 K. The rms error is less than 4 % and the maximum absolute error is less than 10 % over the entire data set. The values of the extracted parameters used in these simulations are given in the proposed model part of Table 2.1. The values for n and γ

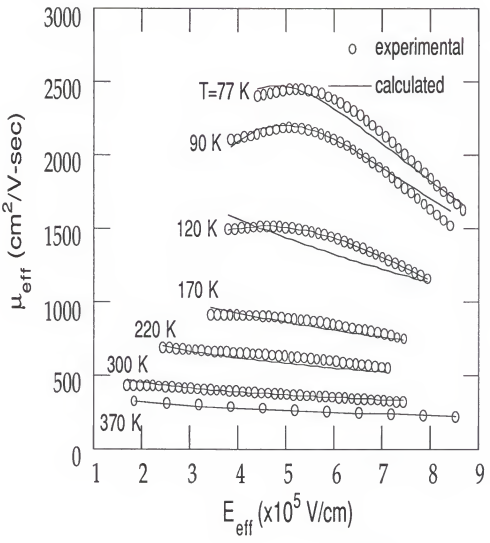


Fig. 2.2 Experimental and simulated electron channel mobility as a function of transverse electric field and temperature for the test MOSFET.

extracted at the 300 K are used for the high temperature simulations and are similar to the values taken from the literature [Eza74]. However, a_c, a_p,and a_s are derived from optimization described in the previous section. Despite the temperature-dependent optimization, a_p and a_s are almost independent of temperature. This can be seen from Table 2.1. The initial estimate of a_p is almost the same as the final optimized value and a_s is roughly a factor of 2 different. Because the changes in magnitude of a_p and a_s are relatively small, we conclude that the reciprocal addition of these scattering mobilities is an acceptable assumption, and the models which we use for phonon and surface roughness scattering are generally accurate.

Some room temperature data taken from Sun and Plummer [Sun80b] have been simulated using the proposed model to see if this model is generally applicable and if the sensitivity of the parameters a_c and a_s to the differences in oxide charge density and surface roughness, respectively, is reasonable. A good fit to the data is shown in the Fig. 2.3 (a) and (c). The parameter a_c shown in Fig. 2.3 (b) which is extracted from the data in Fig. 2 3(a) is roughly a linear function of the oxide charge density as predicted by (2.2). The parameter a_s (in (2.13)) extracted from Fig. 2.3 (c) also shows expected trends. The device having the wet gate oxide has a rougher surface than the device having a dry gate oxide [Sun80b]. From the simulations, a_s is much smaller for the latter device. All parameters taken from this data have been

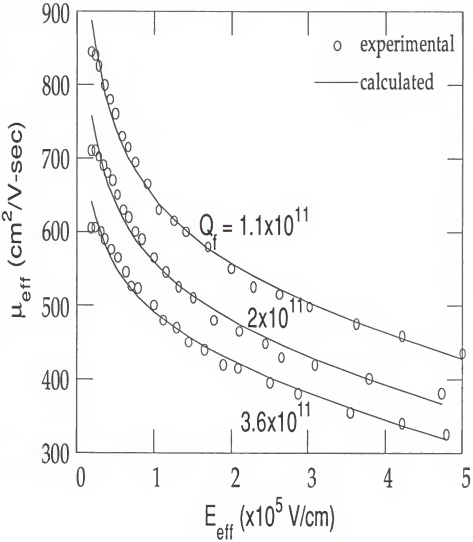


Fig. 2.3 (a) Simulated and experimental electron channel mobility at room temperature. The experimental data with various values of surface oxide charge density Q_f and substrate doping concentration N_A = 9 x 10^{14} cm^{-3} are taken from Sun and Plummer [Sun80b].

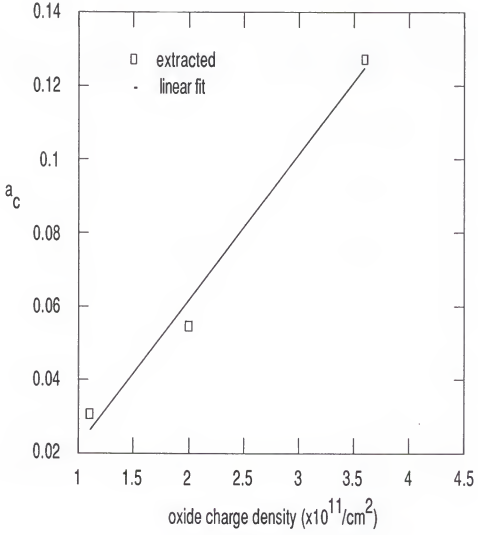


Fig. 2 3(b) The Coulomb scattering mobility parameter a1 of the proposed model extracted from the experimental data in Fig. 2(a) versus surface oxide charge density Q_F.

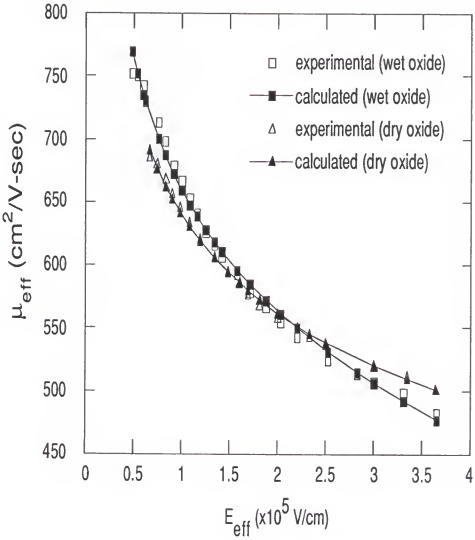


Fig. 2 3(c) Simulated and experimental electron channel mobility at room temperature. The experimental data for MOSFETs with wet gate oxide or dry gate oxide are taken from Sun and Plummer [Sun80b].

extracted assuming the n and γ given in Table 2.1 for the high temperature model because of the identical substrate orientation (100).

In Fig. 2.4, the experimental data is presented together with simulated data using the proposed model and the model of Arora et al. [Aro87]. The discrepancy between the simulations is attributed to differences in the models for the scattering mechanisms and differences in the empiricism. Arora et al. assume that phonon scattering is the predominant mechanism for T > 200 K, and they model the mobility as a function of effective electric field by a commonly used empirical formula. The effective electric field dependence of the Coulomb scattering which arises from carrier screening is not included in their low-temperature (T < 200 K) model. In addition, the field dependence of surface roughness scattering in their low-temperature model has a power m > 1 which is extracted. The rms error is 9 % and the maximum absolute error is 25 % over the entire temperature range between the experimental data and the simulated data from Arora et al.

The proposed model can be simplified by making an assumption about phonon scattering at low temperatures. For example, one assumption might be that phonon scattering can be ignored below 100 K, because its effect is less important than that of Coulomb and surface roughness scattering. The resulting simulations which are as good as that of the unsimplified model are given in Fig. 2.5. The model

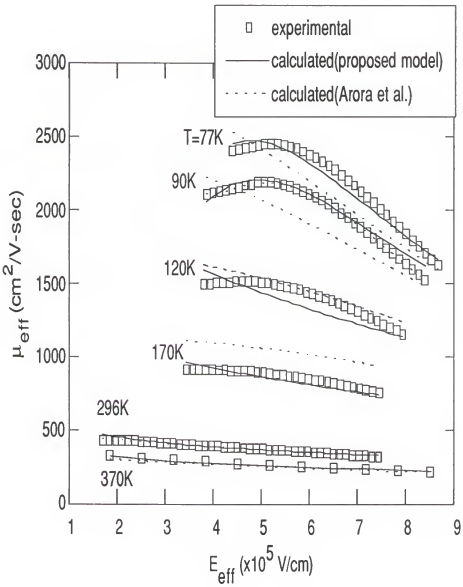


Fig. 2.4 Simulated electron channel mobility as a function of transverse electric field and temperature using the extracted parameters in Table 2.1 for the Arora et al.'s model [Aro87] and for the proposed model. The experimental data are the same as in Fig. 2.2.

Table 2.1

The extracted value of Model Parameters

Proposed model	Simplified Model	Arora et al.[Aro87]
(100K < T ≤ 370K)	(200K < T ≤ 370K)	(200K < T ≤ 370K)
$a_c = 6.68 \times 10^{-8}$	$a_c = 3.84 \times 10^{-3}$	$T_r = 296K$
$a_p = 1.82 \times 10^{-8}$	$a_p = 1.80 \times 10^{-8}$	$\mu_o(T_r) = 495.05$
$a_s = 3.27 \times 10^{-16}$	$a_s = 4.25 \times 10^{-16}$	$\theta(T_r) = 6.91 \times 10^{-7}$
$n = 1.62$	$n = 1.62$	$n = 1.64$
$\gamma = 4.89$	$\gamma = 4.89$	
(77K ≤ T < 100K)	(77K ≤ T < 200K)	(77K ≤ T < 200K)
$a_c = 6.38 \times 10^{5}$	$a_c = 1.60 \times 10^{5}$	$T_r = 296K$
$a_p = 2.65 \times 10^{-8}$	$a_p = 1.56 \times 10^{-8}$	$\mu_o(T_r) = 495.05$
$a_s = 4.89 \times 10^{-16}$	$a_s = 3.54 \times 10^{-16}$	$\theta_1 = 1.58 \times 10^{-12}$
$\alpha = 2.04$	$\alpha = 2.00$	$\theta_2 = 9.90 \times 10^{-5}$
	$n = 1.62$	$m = 2.57$
	$\gamma = 4.89$	$n = 1.17$
Simplification to the proposed model (77K ≤ T < 100K)		
$a_c = 2.62$		
$a_s = 6.21 \times 10^{-16}$		
$\alpha = 1.04$		

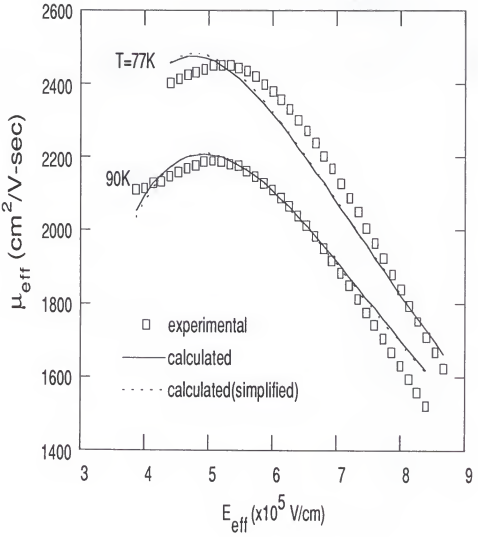


Fig. 2.5 Experimental and simulated electron channel mobility as a function of transverse electric field at T = 77, 90 K. Simulations are done by simplified model which only has Coulomb and surface roughness scattering (parameters are in lower part of the first column of Table 2.1) and the proposed model.

parameters are given in lower part of the proposed model of Table 2.1. However this simplification is not physically justified. Therefore another simplification might be obtained by using the phonon scattering term with the same n and γ extracted at the high temperatures for the low temperature phonon scattering. The simulations from this simplified model are given in the Fig. 2.6 with the experimental data (see the second column of the Table 2.1 for extracted parameters). The goodness of the fit is sufficient for $T > 100$ K, but is not as good as the other simplification for $T < 100$ K.

2.6 Summary

A physically based semi-empirical model for electron mobilities in the MOSFET inversion layers at low longitudinal electric fields has been presented. The model is a reciprocal sum of the same scattering mechanisms used in other models, i.e. phonon, Coulomb, and surface roughness scattering. However, it is more physically based than those models. The functional dependencies of the different scattering mechanisms on the temperature and transverse electric field are more accurate and less empirical. Determination of the experimental mobility data for $77 \text{ K} < T < 370 \text{ K}$ and parameter extraction for the model has been outlined. The proposed model has been demonstrated to adequately simulate the experimental data. The implicit dependencies of the extracted parameters on oxide charge density and surface roughness at

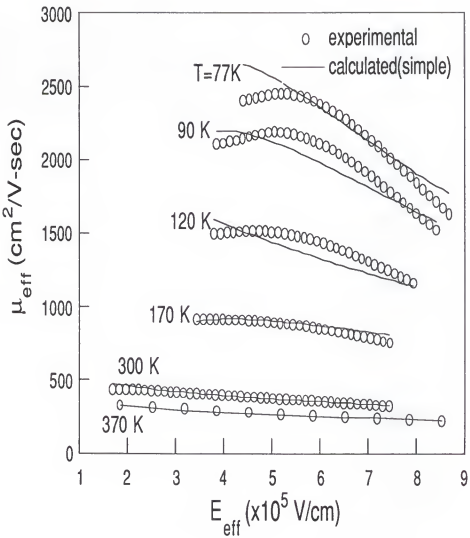


Fig. 2.6 Experimental and simulated electron channel mobility as a function of transverse electric field and temperature. Simulations are done by simplified model which has identical phonon scattering term over the entire temperature range (parameters are in the second column of Table 2.1).

the $Si-SiO_2$ interface give the expected trends. The differences in the scattering mechanisms incorporated into the proposed model and the model of Arora et al. [Aro87] is exemplified by the resulting simulations of the experimental data. Simplifications to the proposed model are also briefly considered.

CHAPTER 3
TEMPERATURE DEPENDENCE OF SOI MOSFET

3.1 Introduction

At high temperature, there are many changes in device parameters from those at room temperature. These are 1) the variation of the threshold voltage with temperature, 2) the increase of leakage current due to increased thermal generation of electron-hole pairs at high temperature, 3) channel mobility degradation at high temperature, and 4) the reduction of generation due to impact ionization at high temperature, etc. In general, the device characteristics become degraded at high temperature except for the impact ionization which is reduced at high temperature. The reduction of impact ionization at high temperature makes the kink in the I_D-V_D characteristic to occur at higher drain bias which is desirable. However, thin-film SOI MOSFET is more resistant to these degradations than bulk MOSFET because it has less variation in threshold voltage and smaller leakage current due to the smaller junction area and thin body film. To account for these temperature dependences, models for several device parameters are presented and these are implemented into SPICE2 [Nag75] which has already included the thin-film SOI MOSFET model for room temperature operation [Vee88]. Through measurements and simulations, the models are

verified and predicts successfully temperature dependences discussed.

3.2 Temperature Dependence

3.2.1 Intrinsic Carrier Density

Temperature dependences of threshold voltage at front channel and thermal generation current or recombination current in the body-drain and body-source junctions are directly related to the temperature dependence of intrinsic carrier density. n_i is given [Sze81],

$$n_i = 4.9 \times 10^{15} \left(\frac{m_n^* m_p^*}{m_o^2}\right)^{0.75} T^{1.5} \exp\left(\frac{-E_g}{2kT}\right) \qquad (3.1)$$

where T is temperature in K, E_g is energy band gap, and k is Boltzmann constant. The effective mass for electron m^*_n or hole m^*_p is modeled in (3.2), (3.3) by the fit to the experimental data of Barber [Bar71].

$$m_n^* = m_o \left(1.034 + 5.826 \times 10^{-4} T - 2.826 \times 10^{-7} T^2\right) \qquad (3.2)$$

$$m_p^* = m_o \left(0.552 + 1.1 \times 10^{-3} T - 7.769 \times 10^{-7} T^2\right) \qquad (3.3)$$

The temperature dependence for the bandgap E_g in (3.4) is taken from the result of Blaudau et al. [Bla74].

$$E_g = 1.179 - 9.025 \times 10^{-5} T - 3.050 \times 10^{-7} T^2 \qquad (3.4)$$

As can be seen in (3.1), the intrinsic carrier density increases exponentially with increasing temperature. Therefore, the channel doping density should be large enough to be greater than n_i over the whole range of operating temperature in order for carrier concentration to be controlled by doping rather than by thermal generation of electron-hole pair.

3.2.2 Threshold Voltage

The temperature dependence of threshold voltage of front gate for possible three cases of device operation in SOI MOSFET will be investigated and comparison of the variation of threshold voltage with temperature between the cases will be made. The three cases are TFA (back surface accumulation) mode and TFD (back surface depletion) mode in thin-film device in which the body-film is fully depleted at strong inversion of front channel. and thick-film device case where the body-film is thick, so it is never fully depleted at strong inversion of front channel. The threshold voltage of the front gate, V_{Tf}, for thin-film n-channel SOI MOSFET which has long channel-length is given by Lim et al. [Lim85],

$$V_{Tf} = V_{FB}^{f} + (1 + \alpha)\, 2\phi_B - \frac{Q_b}{2\, C_{of}} - \frac{C_b}{C_{of}} V_{BS} \qquad \text{(TFA)}$$

$$= V_{FB}^{f} + 2\phi_B - \frac{Q_b}{2\, C_{of}} - \alpha \left(V_{GBS} - V_{FB}^{b} - 2\phi_B + \frac{Q_b}{2\, C_{ob}} \right) \text{(TFD)} \qquad (3.5)$$

V^{f}_{FB} or V^{b}_{FB} is front and back gate flat-band voltage, C_b Δ

ε_s/t_b, C_{of} is ε_{ox}/t_{of}, C_{ob} is ε_{ox}/t_{ob}, and ε_s or ε_{ox} is permittivity of Si or SiO_2, and t_b, t_{of} , or t_{ob} is thicknesses of the body film, the front or back gate oxide, ϕ_B is Fermi potential of the neutral body film, $Q_b \Delta -qN_A t_b$, $C_{ob} = \varepsilon_{ox}/t_{ob}$, V_{BS} and V_{GbS} are body and back gate bias, and

$$\alpha = \frac{C_b}{C_{of}} \qquad \text{(TFA)}$$

$$= \frac{\dfrac{C_{ob}\, C_b}{C_{ob} + C_b}}{C_{of}} \qquad \text{(TFD)} \qquad (3.6)$$

For a n-channel SOI MOSFET which has a body-film too thick to be fully depleted by any combination of gate biases, and, consequently, has a partially depleted body, the threshold voltage is given by that of bulk MOSFET [Sze81],

$$V_{Tf} = V_{FB}^f + 2\phi_B + \frac{\sqrt{2\varepsilon_s qN_A(2\phi_B - V_{BS})}}{C_{of}} \quad \text{(thick-film)} \qquad (3.7)$$

Before investigating temperature dependence of V_{Tf}, let us consider some points about threshold voltage at room temperature. The magnitude of V_{Tf} for TFA is always larger than that for TFD and is equal to or larger than that for the thick-film case, depending on the body-film thickness. These differences in V_{Tf} come from the difference in electric field at the front surface edge of the depletion region E_{sf}, as will be discussed later. The threshold voltage at the front gate

V_{Tf} can be expressed as below when the source and body is tied, i.e. $V_{BS} = 0$ V,

$$V_{Tf} = \psi_{sf} \left(= 2\phi_B\right) + \psi_{of} \left(\text{when } \psi_{sf} = 2\phi_B\right) + \Phi^f_{MS} \tag{3.8}$$

where ψ_{sf} is front surface potential and $= 2\phi_B$, ψ_{of} is potential drop across front gate oxide, and Φ^f_{MS} is work function difference between front gate and body-film. In (3.8), we will have the same ψ_{sf} and Φ^f_{MS} value for the three cases at threshold if we have the same thickness of front gate oxide, the same front gate metal, and the same body doping concentration. This is not the case for ψ_{of}, because it depends on bias conditions at back gate and body-film thickness. ψ_{of} is related to E_{sf} as below by the electric field boundary condition between front gate oxide and body-film, assuming no oxide charge and no inversion layer charge,

$$\psi_{of} = \frac{\varepsilon_s E_{sf}}{C_{of}} \tag{3.9}$$

Now, for the thin-film device, E_{sf}, taken from integration of Poisson's equation across the film [Lim83], is

$$E_{sf} = \frac{\psi_{sf} - \psi_{sb}}{t_b} + \frac{q N_A t_b}{2 \varepsilon_s} \tag{3.10}$$

where ψ_{sb} is back surface potential. E_{sf} of thick-film device

at strong inversion is given by bulk MOSFET theory [Sze81],

$$E_{sf} = \frac{q\ N_A\ x_{d(max)}}{\varepsilon_s} \quad \text{(thick-film at strong inversion)} \tag{3.11}$$

where $x_{d(max)}$ is maximum depletion width and is

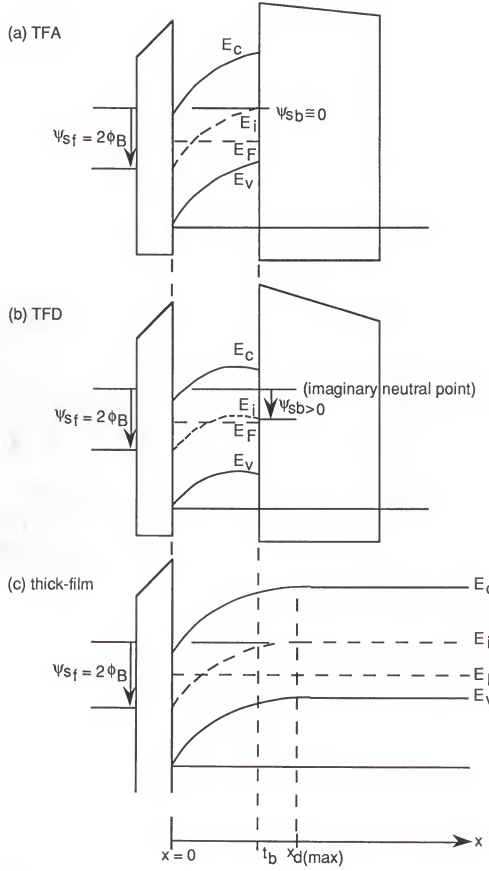
$$x_{d(max)} = \sqrt{\frac{4\ \varepsilon_s\ \phi_B}{q\ N_A}} \tag{3.12}$$

Now, from (3.8)-(3.11), it is seen that the difference in E_{sf} is the reason for the different V_{Tf} for the TFA, TFD, and thick-film case. In TFA case where back surface potential is pinned to zero, $\psi_{sb} \cong 0$ and $\psi_{sf} = 2\phi_B$, so from (3.10) at strong inversion,

$$E_{sf} = \frac{2\ \phi_B}{t_b} + \frac{q\ N_A\ t_b}{2\ \varepsilon_s} \quad \text{(TFA at strong inversion)} \tag{3.13}$$

From (3.11), (3.13), when $t_b = x_{d(max)}$, E_{sf} for TFA at strong inversion is the same as that of thick-film at strong inversion. Therefore, V_{Tf} of TFA is the same as that of thick-film case when $t_b = x_{d(max)}$. When $t_b < x_{d(max)}$ (it is a normal situation), V_{Tf} of TFA is larger than that of thick-film device due to the larger E_{sf} as can be seen in (3.11) and (3.13) and as visualized in Fig. 3.1. In Fig. 3.1, when $t_b < x_{d(max)}$, the slope of the band edges E_c or E_v for TFA is steeper than that of thick-film device because the band

Fig. 3.1 Energy Band Diagram for (a) TFA (back surface accumulation) case and (b) TFD (back surface depletion) case of thin-film device, and (c) thick-film device at strong inversion of front channel.


(a) TFA
E_c
$\psi_{sb} \cong 0$
E_i
$\psi_{sf} = 2\phi_B$
E_F
E_v
(b) TFD
E_c
(imaginary neutral point)
E_i
$\psi_{sb>0}$
$\psi_{sf} = 2\phi_B$
E_F
E_v
(c) thick-film
E_c
E_i
$\psi_{sf} = 2\phi_B$
E_F
E_v
x
x = 0
t_b
$x_{d(max)}$

edges for TFA must be bent by same amount in a shorter distance (t_b) for front surface potential to become the same vaule of $2\phi_B$ as thick-film device. The slope of the band bending is E_{sf} multiplied by q. Note that as t_b becomes smaller, V_{Tf} of TFA becomes larger due to the increase of E_{sf} as can be seen in (3.13) or in Fig. 3.1. In TFD case where back surface potential $\psi_{sb} > 0$, therefore with $\psi_{sf} = 2\phi_B$ at strong inversion, in (3.10) E_{sf} is smaller than that of TFA case as can be seen Fig. 3.1, so is V_{Tf} of TFD case.

The temperature dependence of V_{Tf} comes from the temperature dependences of ϕ_B, V^f_{FB}, V^b_{FB}. For the temperature dependence of ϕ_B,

$$\phi_B = \frac{kT}{q} \ln \left(\frac{N_A}{n_i}\right) \tag{3.14}$$

The temperature dependences of V^f_{FB} and V^b_{FB} are attributed to temperature dependences of the work function difference Φ_{MS} between front or back gate and body film which is dependent on ϕ_B. For n-channel device with the n^+ polysilicon front gate which is usual for surface channel devices,

$$\begin{aligned} \Phi^f_{MS} &= \frac{1}{q}\left(E_c - E_{F(\text{front gate})}\right) - \frac{1}{q}\left(E_c - E_{F(\text{body})}\right) \\ &= -\frac{kT}{q} \ln \frac{N_{gate}}{n_i} - \frac{kT}{q} \ln \frac{N_A}{n_i} \\ &= -\frac{kT}{q} \ln \frac{N_{gate}}{N_A} \end{aligned} \tag{3.15}$$

where $E_{F(front\ gate)}$, $E_{F(body)}$ is Fermi level at the polysilicon gate or body-film, respectively, and N_{gate} is the doping concentration of the polysilicon gate. For n-channel device with aluminum gate,

$$\Phi_{MS}^{f} = 4.1 - \left(4.05 + \frac{E_g}{2\,q} + \phi_B\right) \tag{3.16}$$

For the back gate of n-channel with n-type subtrate,

$$\Phi_{MS}^{b} = -\frac{kT}{q} \ln \frac{N_{substrate}}{n_i} - \frac{kT}{q} \ln \frac{N_A}{n_i}$$

$$= -\frac{kT}{q} \ln \frac{N_{substrate}}{N_A} \tag{3.17}$$

where $N_{substrate}$ is doping concentration of substrate.

The expression for the variation in threshold voltage with temperature can be obtained by taking derivatives of (3.5) and (3.7) with respect to temperature. The results are

$$\frac{\partial V_{Tf}}{\partial T} = \frac{\partial \Phi_{MS}^{f}}{\partial T} + 2\,(1 + \alpha)\,\frac{d\phi_B}{dT} \qquad \text{(TFA)}$$

$$= \frac{\partial \Phi_{MS}^{f}}{\partial T} + 2\,\frac{d\phi_B}{dT} + \alpha\left(2\,\frac{d\phi_B}{dT} + \frac{\partial \Phi_{MS}^{b}}{\partial T}\right) \qquad \text{(TFD)} \tag{3.18}$$

$$= \frac{\partial \Phi_{MS}^{f}}{\partial T} + \left(2 + \frac{\sqrt{\varepsilon_s\, q\, N_A}}{C_{ox}\sqrt{\phi_B}}\right)\frac{d\phi_B}{dT} \qquad \text{(thick-film)}$$

Now, from (3.15),

$$\frac{\partial \Phi^{f}_{MS}}{\partial T} = - \frac{k}{q} \ln \frac{N_{gate}}{N_A} \tag{3.19}$$

for the n+ poly S_i gate, so the variation of flat-band voltage of the poly S_i gate with temperature is due to the difference of doping concentration of the gate and body-film, if these two is same from (3.13), $\partial \Phi^{f}_{MS}/\partial T$ becomes zero. From (3.14),

$$\frac{\partial \phi_B}{\partial T} = \frac{k}{q} \left(\ln\left(\frac{N_A}{n_i}\right) - 2 \frac{T}{n_i} \frac{\partial n_i}{\partial T} \right) \tag{3.20}$$

and $\partial \phi_B/\partial T < 0$, because $\partial n_i/\partial T$ is an exponentially increasing function of T as can be seen in (3.1).

Let us compare the variation of threshold voltage with temperature between the three cases. From (3.8),

$$\frac{\partial V_{Tf}}{\partial T} = 2 \frac{\partial \phi_B}{\partial T} + \frac{\partial \psi_{of}}{\partial T} + \frac{\partial \Phi^{f}_{MS}}{\partial T} \tag{3.21}$$

In (3.21), $\partial \phi_B/\partial T$ and $\partial \Phi^{f}_{MS}/\partial T$ are the same for all cases if they have same gate oxide thickness, same front gate material, and same doping concentration for the body film. It is $\partial \psi_{of}/\partial T$ due to the difference of $\partial E_{sf}/\partial T$ that causes $\partial V_{Tf}/\partial T$ to be different among the cases. From (3.10) and (3.11), $\partial E_{sf}/\partial T$ at strong inversion of front channel is given by,

$$\frac{\partial E_{sf}}{\partial T} = \frac{2}{t_b}\frac{\partial \phi_B}{\partial T} \quad \text{(TFA)}$$

$$= \left(\frac{2}{t_b}\frac{\partial \phi_B}{\partial T} - \frac{1}{t_b}\frac{\partial \psi_{sb}}{\partial T}\right) \quad \text{(TFD)} \qquad (3.22)$$

$$= \frac{2}{x_{d(max)}}\frac{\partial \phi_B}{\partial T} \quad \text{(thick-film)}$$

In (3.22), when $x_{d(max)} = t_b$, $\partial E_{sf}/\partial T$ of TFA becomes equal to $\partial E_{sf}/\partial T$ of thick-film case, so does $\partial V_{Tf}/\partial T$ of TFA. However, normally $x_{d(max)} > t_b$, therefore $|\partial E_{sf}/\partial T|$ of TFA > $|\partial E_{sf}/\partial T|$ of thick-film case, so $|\partial V_{Tf}/\partial T|$ of TFA > $|\partial V_{Tf}/\partial T|$ of thick-film case. Note $\partial E_{sf}/\partial T$ and $\partial V_{Tf}/\partial T$ have negative values. In TFD mode ψ_{sb} is given [Lim83]

$$\psi_{sb} = \frac{V_{GbS} - V_{FB}^{b} + \frac{C_b}{C_{ob}}\psi_{sf} + \frac{Q_b}{2C_{ob}}}{1 + \frac{C_b}{C_{ob}}} \qquad (3.23)$$

From (3.23),

$$\frac{\partial \psi_{sb}}{\partial T} \cong \frac{\frac{C_b}{C_{ob}}\frac{\partial \psi_{sf}}{\partial T}}{1 + \frac{C_b}{C_{ob}}}$$

$$\cong \frac{\partial \psi_{sf}}{\partial T} \qquad (3.24)$$

because normally $C_b/C_{ob} >> 1$. Now, from (3.22), $\partial Esf/\partial T \cong 0$ for TFD, where $\psi_{sf} = 2\phi_B$ at threshold. Therefore $|\partial V_{Tf}/\partial T|$ of TFD is

the smallest of the three cases. In conclusion, differences in $\partial V_{Tf}/\partial T$ between TFA, TFD, and thick-film case are due to different temperature dependence of E_{sf}. We can have the smallest $|\partial V_{Tf}/\partial T|$ from the TFD case. These can be seen also from (3.18) because α of TFA is very large while α of TFD is small.

The maximum depletion region width, $x_{d(max)}$, which is in (3.12), decreases with increasing temperature due to the decrease of ϕ_B. Therefore, if the device is to operate in the thin-film or fully depleted mode at high temperature, the body thickness and body doping density have to be chosen considering this fact. Otherwise, the device will be in the thick-film or partially depleted mode at high temperature, even if it can be operated in thin-film mode at room temperature.

3.2.3 Leakage Current

The leakage current due to thermal generation at the reverse-biased body-drain junction and depleted body-film of SOI MOSFET is temperature-dependent due to the temperature dependence of thermal generation and generation lifetime. The leakage current due to thermal generation or impact ionization flows through the source-body junction by recombination. The recombination current is also temperature-dependent due to the temperature dependence of intrinsic carrier density and recombination lifetime. The device structure considered has the source and drain

diffusions bottomed at the underlying buried oxide layer as seen in Fig. 1.1.

3.2.3.1 Thermal Generation Current

There are three important thermal generation current component which will be considered. First, the current due to thermal generation inside space charge region of the reverse-biased body-drain junction. Second, the current due to thermal generation at the edge of neutral body just outside of space charge region of reverse-biased body-drain junction. This current is called usually diffusion current. Finally, the current due to thermal generation in the depleted body-film.

Let us think about the first current component. This current is given [Sze81]

$$I_{gen,scr} = \frac{q\, n_i W_i}{\tau_g}\, t_b\, Z \tag{3.25}$$

where Z is channel width. τ_g is effective generation lifetime inside space charge region of the reverse-biased body-drain junction. Here W_i is a portion of space charge region where the generation is maximum; outside of it the generation is negligible. In W_i, p and n << n_i and W_i is given [Cal72]

$$W_i = \sqrt{\frac{2\,\varepsilon_s\, kT}{q^2\, N_A}} \left[\sqrt{\ln\left(\frac{N_A}{n_i}\right) - \frac{q\, V_{BD}}{kT}} - \sqrt{\ln\left(\frac{N_A}{n_i}\right)} \right] \tag{3.26}$$

The second current component is due to thermal generation at the edge of neutral body-film just outside of the space charge region in the reverse-biased body-drain junction. This current is usually called diffusion current and expressed by ideal diode current equation. In a SOI MOSFET which has thick body-film, this current always contribues to leakage current. However, even in a SOI MOSFET which has thin body-film, this current should be considered because in the subthreshold when the body-film is not fully depleted or in the off state of the device, there is undepleted body-film region where thermal generation will occur. The current which is governed by the ideal diode current relation and which depends on the size of the undepleted region in the body film, is expressed

$$I_{diff} = q \sqrt{\frac{D_n}{\tau_r}} \frac{n_i^2}{N_A} \left(\exp\left(\frac{q\ V_{BD}}{kT}\right) - 1\right)\left(t_b - x_d(L)\right) Z \qquad (3.27)$$

where D_n is electron diffusivity, and τ_r is recombination lifetime in neutral body region which can be given by SRH recombination theory because of the low doping density of body film. $x_d(L)$ is depletion region width at the drain end of the channel.

The depletion region width $x_d(y)$ is given [Sze81]

$$x_d(y) = \sqrt{\frac{2\ \varepsilon_s \left(\phi_s + V_y(y)\right)}{q\ N_A}} \qquad (3.28)$$

where $V_y(y)$ is potential difference between a point y along the channel and the neutral body-film. The front surface potential ϕ_s in (3.28) is approximated to be piecewisely linear in V_{GfS} (see Fig. 3.2) using the relationship between ϕ_s and V_{GfS} in the literature [Bre81], i.e,

$$\phi_s = \frac{V_{GfS} - V_{FB}^f}{V_{Tf} - V_{FB}^f} 2\phi_B \qquad \text{for } V_{GfS} < V_{Tf}$$
$$= 2\phi_B \qquad \text{for } V_{GfS} \geq V_{Tf} \quad . \tag{3.29}$$

Note in (3.29) when $V_{GfS} = V_{Tf}$, $\phi_s = 2\phi_B$.

Now, let us think about the current due to thermal generation in the depleted body-film. In the depleted body-film, there will be net generation of electron-hole pairs and this generation will be temperature-dependent. The generated electrons are swept to the drain and the generated holes are attracted to the neutral region in the body, therefore the current due to thermal generation in the depleted body flows from drain to the body. This current is formulated in a similar way to the current due to thermal generation inside the space charge region and given

$$I_{gen,dep} = \frac{q\, n_i}{\tau_g} \left(\frac{(W_i(0) + W_i(L))}{2} \right) L\, Z \tag{3.30}$$

where L is channel length and τ_g is assumed to be the same as the one in (3.25). $W_i(0)$ and $W_i(L)$ is a portion of depleted

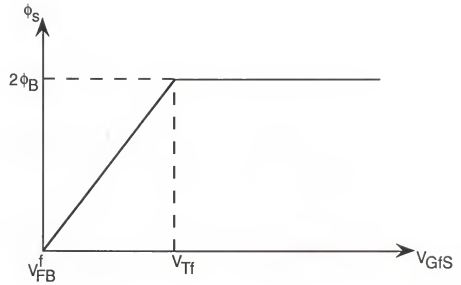


Fig. 3.2 Surface potential ϕ_s of n-channel MOSFET as a piecewise-linear function of front gate voltage V_{GfS}.

body-film where the thermal generation rate is maximum and outside of it the rate is negligible at the source and drain end of body-film, respectively. Therefore, $(W_i(0) + W_i(L))L/2$ is an approximated area (which can be triangular or trapezoidal depending on the $W_i(0)$) inside the depleted body-film where the thermal generation rate is maximum. $W_i(y)$ is given

$$W_i(y) = x_d(y) \frac{\left(\sqrt{\phi_B + V_y(y)} - \sqrt{\phi_B}\right)}{\sqrt{\phi_s}} \qquad \text{(thick-film)}$$

$$= \frac{\varepsilon_s}{q N_A} \left(\sqrt{E_{sf}^2 - \frac{2qN_A}{\varepsilon_s}\left(\psi_{sf} - \phi_B - V_y(y)\right)} - \sqrt{E_{sf}^2 - \frac{2qN_A}{\varepsilon_s}\left(\psi_{sf} - \phi_B\right)} \right) \qquad \text{(thin-film)} \qquad (3.31)$$

where $V_y(0) = -V_{BS}$, $V_y(L) = -V_{BD}$. (For the derivation of (3.31), see the Appendix A.)

3.2.3.2 Recombination Current

The current due to thermal generation in the body-drain junction and the depleted body-film and due to impact ionization at the drain end flows from body to source by recombination in the neutral body-film, inside the space charge region of the source-body junction, or in the neutral source because the body is floated in SOI MOSFET First, let us investigate the current by the recombination inside the space charge region of source-body junction. By SRH theory which is applicable due to the low doping density of the

body-film, this current is given [Sze81]

$$I_{rec,scr} \cong \frac{q\ n_i\ W_{scr}}{\tau_{r,scr}} \exp\left(\frac{q\ V_{BS}}{2\ kT}\right) t_b\ Z \qquad (3.32)$$

where W_{scr} is space charge region width, and $\tau_{r(scr)}$ is effective recombination lifetime inside the space charge region of forward biased source-body junction. In (3.32), the region where recombination rate is maximum inside the space charge region is approximated by W_{scr}.

There is another place where recombination occurs. It is the neutral body region. The current by this recombination can be expressed by ideal diode current equation. Now, the size of the neutral body region must be considered, because it depends on the gate bias and the thickness of body-film. The current is given

$$I_{rec,body} = q \sqrt{\frac{D_n}{\tau_r}} \frac{n_i^2}{N_A} \left(\exp\left(\frac{q\ V_{BS}}{k\ T}\right) - 1\right)(t_b - x_d(0))\ Z \qquad (3.33)$$

where $x_d(0) = x_d(y)$ when $y = 0$ and τ_r is recombination lifetime in the undepleted body region which can be given by SRH recombination theory because of the low doping density of body film.

In the TFD case, the energy barrier between the source and the body-film is so low that the holes easily diffuse to the source and recombine with electrons there [Yos89]. This can be a dominant factor for TFD. The current can be

expressed a minority-carrier recombination current in the heavily doped region. Here the dominant recombimation mechanism is Auger band-to-band recombination because the source is heavily doped. This current can be given by Fossum et al. [Fos81],

$$I_{rec,source} = \frac{qn_i^2}{N_{D(eff)}} \left(\frac{1}{S_p} + \frac{1}{D_{po}/W_H} \right)^{-1} \left(1 + \frac{\tau_t}{\bar{\tau}_A} \right) \exp\left(\frac{qV_{BS}}{kT} \right) \qquad (3.34)$$

where $N_{D(eff)}$ = effective doping density in the source,

S_p = surface recombination velocity for hole,

D_{po} = hole diffusion constant at the interface between front gate oxide and the body-film,

W_H = effective depth of the neutral source region,

τ_t = hole transit trime, and

$\bar{\tau}_A$ = average Auger hole lifetime.

3.2.3.3 Temperature Dependence of Parameters

The temperature dependence of thermal generation current and recombination current discussed so far is attributed to those of n_i, D_n, τ_r, $\tau_{r(scr)}$, τ_g, $x_d(y)$, W_{scr}, W_i, and $W_i(y)$. The temperature dependence of n_i was already presented. The temperature dependence of diffusivity D_n can be traced from Einstein relation, $D_n = \mu_{nb}\, kT/q$, where μ_{nb} is bulk electron mobility which depends on temperature. W_{scr} depends on $\phi_B(T)$.

The recombination lifetime in the neutral body region, τ_r in (3.33) is equal to τ_{no} of SRH theory under the assumptions that excess carriers are in low-injection level and the trap

energy level E_T is equal to intrinsic Fermi level E_i. These assumptions are reasonable for the normal SOI MOSFET. The effective recombination lifetime in the space charge region, $\tau_{r(scr)}$, is $2\sqrt{\tau_{no}\tau_{po}}$ [Sze 81]. From SRH theory,

$$\tau_{xo} = \frac{1}{v_{th}\ \sigma_x\ N_T} \tag{3.35}$$

where the subscripts x is n for electrons and is p for holes, v_{th} is the thermal velocity proportional to $\sqrt{T}$, σ_n and σ_p are capture cross-sections for electrons and holes proportional to $T^{-2.7}$ and $T^{-3.3}$ [Tya83], respectively, and N_T is trap density which is temperature-independent. Therefore, the temperature dependence of τ_{no} and τ_{po} can be modeled using the above relations as

$$\tau_{xo}(T) = \tau_{xo}(300)\left(\frac{T}{300}\right)^m \tag{3.36}$$

where for electrons, m = 2.2, and for holes, m = 2.8. The temperature dependence of $\tau_{r(scr)}$ can be obtained using (3.36),

$$\begin{aligned}\tau_{r(scr)}(T) &= 2\sqrt{\tau_{no}(T)\tau_{po}(T)} \\ &\cong 2\tau_{no}(300)\left(\frac{T}{300}\right)^{2.5}\end{aligned} \tag{3.37}$$

where $\tau_{no}(300)$ is assumed to be equal to $\tau_{po}(300)$.

The generation lifetime τ_g inside the space charge region of reverse-biased body-drain junction is given by the result of Schroder [Sch82], which is based on SRH recombination theory,

$$\tau_g = 2\tau_{no}\sqrt{\frac{\sigma_n}{\sigma_p}}\cosh\left[\frac{(E_T - E_i)}{kT}\right] \tag{3.38}$$

Here $\tau_{no}\sqrt{\sigma_n/\sigma_p}=1/\left(V_{th}N_T\sqrt{\sigma_n/\sigma_p}\right) \propto T^{2.55}$. Therefore, τ_g is modeled as

$$\tau_g = \tau_a T^{2.55}\cosh\left(\frac{\tau_b}{T}\right) \tag{3.39}$$

where τ_a is a temperature independent parameter, $\tau_b = (E_T - E_i)/k$, and both τ_a and τ_b are process dependent. Using (3.25), we can extract τ_g from the measurements of the thermal generation current in the reverse-biased body-drain junction. Then, from the extracted τ_g, τ_a and τ_b are extracted using (3.39). According to literature [Sch84] at room temperature, the generation lifetime in the space charge region is about 10-50 times larger than recombination lifetime in neutral region because the generation lifetime is very sensitive to the energy level of the dominant trap as can be seen in (3.36), but the recombination lifetime is not sensitive that much. Therefore, by using this fact, $\tau_{no}(300)$ can be set as a fraction of τ_g which is determined from measurements.

3.2.4 Channel Mobility

At high temperature, channel mobility becomes smaller due to the increase of scatterings as is seen in Chapter 2. It is surface phonon scattering that is dominant at high temperature and depends strongly on temperature, therefore makes channel mobility to be reduced. The effect of Coulomb scattering on channel mobility is important at low temperature, but is negligible at high temperature because of increased carrier velocity. The surface roughness scattering which becomes important at high electric field is less important to thin-film SOI MOSFET in which the carriers experience smaller vertical electric field than at bulk MOSFET [Stu88, Yos89]. Therefore, channel mobility of electron, $\mu_{eff,n}$, at high temperature can be modeled using the surface phonon scattering term only as in (3.40). (see Chapter 2 on phonon scattering limited mobility.)

$$\mu_{eff,n} = \frac{1}{a_p T^n E_{eff}^{\frac{1}{\gamma}}} \tag{3.40}$$

where E_{eff} is the effective electric field, and a_p, n, and γ are fitting parameters which can be extracted from the room-temperature measurements.

E_{eff} is a function of E_{sf} in (3.10) or (3.11). As discussed earlier, E_{sf} of TFD is smaller than that of TFA and it can be smaller than that of thick-film device depending on back gate bias or ψ_{sb}. Therefore μ_{eff} of TFD is also expected to be larger than μ_{eff} of TFA and can be larger than that of

thick-film device. The measurement results in the literature [Yos88] confirm this.

3.2.5 Current due to Impact Ionization

The generation current due to weak impact ionization in the thin-film SOI MOSFET can be expressed [Vee88]

$$I_{Gi} = (M - 1)\, I_{DS} \,. \tag{3.41}$$

M is the multiplication factor of electron current (in an n-channel device), I_{DS} is channel current. Now,

$$(M - 1) = \frac{\alpha_o}{\beta_o} \left(V_{DS} - V_{DS(sat)}\right) \exp\left[- \frac{\beta_o l_c}{\left(V_{DS} - V_{DS(sat)}\right)} \right] \tag{3.42}$$

where $V_{DS(sat)}$ is the drain saturation voltage and

$$l_c = t_b \left[\frac{C_b\, \beta}{2\, C_{of}\, (1 + \alpha)} \right]^{\frac{1}{2}} \,. \tag{3.43}$$

β is 1 for TFA, or $1 + C_b/(C_b + C_{ob})$ for TFD. The amount of generation current by impact ionization at fixed bias is dependent on temperature because of following reasons. First, channel current is temperature-dependent due to channel mobility degradation and threshold voltage reduction at high temperature as discussed in the previous sections. Therefore, the change of channel current with temperature makes I_{Gi} to become dependent on temperature. Second, threshold voltage

reduction at high temperature makes the drain saturation voltage to become smaller, therefore M becomes temperature-dependent as seen in (3.42) and so does I_{Gi}. Finally, mean free path of carriers decrease as temperature increases because of increased scattering as discussed in Chapter 2. Therefore the number of carrier which has enough energy to make impact ionization at electric field of same strength becomes reduced at high temperature. This makes the coefficients α_o, β_o in (3.42) to become changed with temperature [Sze81], which makes M and I_{Gi} to become temperature-dependent. The coefficients α_o, β_o in (3.42) are from the impact ionization rate which is defined as number of electron-hole pairs generated by impact ionization per unit length of travel of an electron or hole [Sze81]. From the literature [Sel89], the temperature dependence of α_o and β_o can be given

$$\alpha_o = 7x10^5\left(0.57 + 0.43\left(\frac{T}{300}\right)^2\right) \quad . \tag{3.44}$$

$$\beta_o = 1.23x10^6\left(0.625 + 0.375\left(\frac{T}{300}\right)\right) \quad . \tag{3.45}$$

3.3 Discussions And Model Verification

To verify the temperature-dependent model and to show trends, we have measured and simulated long-channel SOI MOSFET. The temperature-dependent models are implemented in the existing thin-film SOI MOSFET model [Vee88] for SPICE2 simulation. The test devices are n-channel MOSFETs built on

SIMOX substrates with a 0.25-μm silicon film thickness and an underlying 0.45-μm silicon-dioxide layer thickness. They have W = 50 μm, L = 25 μm, and channel doping density, N_A = $10^{17}/cm^3$. The source and drain diffusions of the devices are bottomed into the buried oxide layer. Because of the higher channel doping density, the devices with t_b=0.25 μm are bulk-like (thick-film) devices and simulations of the devices are done via the TFA case of the thin-film model with t_b set equal to the depletion-region width, $x_{d(max)}$, at strong inversion as suggested by Fossum et al. [Fos90]. The measurements are done from room temperature up to 200°C which is the measurement limit of the available test environment. However, the simulations are done up to 300°C to show the trends.

3.3.1 Variation in Threshold Voltage

Measurements and simulations of threshold voltage of the front channel V_{Tf} of test devices at several body bias are shown in Fig. 3.3. The test devices have thick body-film (i.e, t_b = 0.182 μm for $N_A = 10^{17}$ cm^{-3}), so the simulations of V_{Tf} have been done by making $t_b = x_{d(max)}$ because V_{Tf} of thick-film becomes equal to V_{Tf} of TFA by doing that from (3.11) and (3.13).

The variation of V_{Tf} with temperature for the cases of TFA, TFD, and thick-film are different due to the different $\partial E_{sf}/\partial T$ as discussed in section 3.2.2. The deviation of V_{Tf} at high temperature from that at room temperature are shown in

Fig. 3.4. For thick-film device, the measured V_{Tf} values of test devices in Fig. 3.3 are used, while for TFA and TFD of thin-film devices simulations are made using same device parameters extracted from test devices except for t_b which is chosen to be 0.07 μm to insure the full depletion of body film at high temperatures. In Fig. 3.4 $|\partial V_{Tf}/\partial T|$ of TFD is the smallest of the three cases, as expected.

Let's consider the effect of t_b on $|\partial V_{Tf}/\partial T|$ in TFA case. As can be seen (3.22), for TFA as t_b becomes smaller, $\partial E_{sf}/\partial T$ becomes smaller, so does $|\partial V_{Tf}/\partial T|$. This is shown from the simulated results in Fig. 3.5. The three devices in Fig. 3.5 have same parameters except for t_b. The device which has smaller t_b has steeper $|\partial V_{Tf}/\partial T|$ slope in the figure as expected and it has larger V_{Tf} value as can be seen in (3.5) and (3.8).

From (3.20), it can be seen that $\partial \phi_B/\partial T$ (in n-channel device) depends on N_A, therefore $|\partial V_{Tf}/\partial T|$ is related to N_A. From (3.20), $\partial \phi_B/\partial T$ is negative value because $\partial n_i(T)/\partial T$ is very large. Therefore when N_A is large, $|\partial \phi_B/\partial T|$ is small and $|\partial V_{Tf}/\partial T|$ is small. The simulated results of the V_{Tf} variation with temperature for the devices having different N_A are shown in Fig. 3.6 for TFA case and Fig. 3.7 for TFD case. In both figures the devices having large N_A show smaller V_{Tf} reduction with temperature increase as expected. In Fig. 3.6 and 3.7, V_{Tf} is larger for devices having greater N_A, of course. Comparing the results in Fig. 3.6 and 3.7, it can be seen that V_{Tf} of TFA case in Fig. 3.6 decreases fast than that

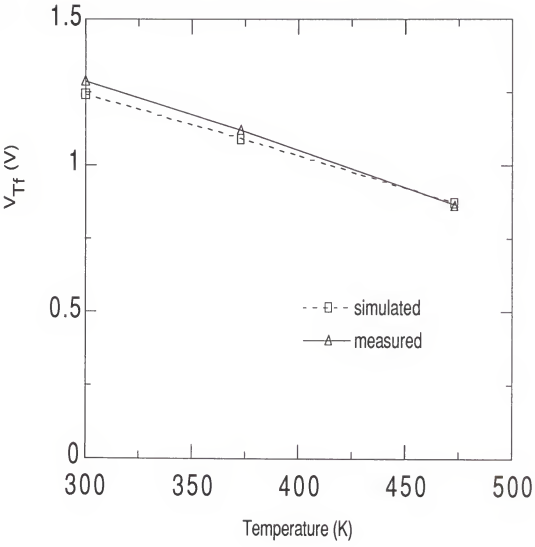


Fig. 3.3 Measured and simulated threshold voltage of front gate V_{Tf} with temperatures for devices with thick-film body (t_b = 0.25mm) and N_{sub} is $10^{17}cm^{-3}$.

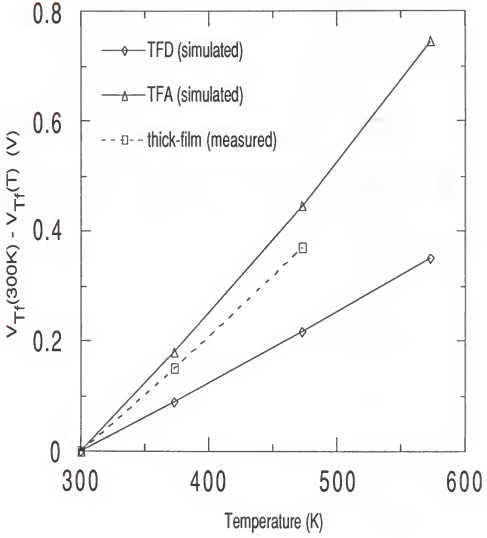


Fig. 3.4 Comparison of variation in threshold voltage V_{Tf} with temperatures for cases of TFA (t_b = 0.07μm), TFD (t_b = 0.07μm), and thick-film (t_b = 0.25μm). N_{sub} is $10^{17}cm^{-3}$. $V_{Tf}(300K)$ is used as a reference point.

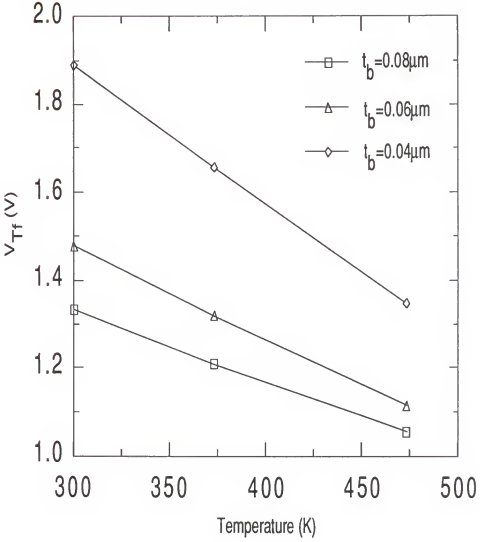


Fig. 3.5 Simulation of variation in threshold voltage of front gate V_{Tf} with temperature for the TFA mode devices having different body-film thickness, t_b.

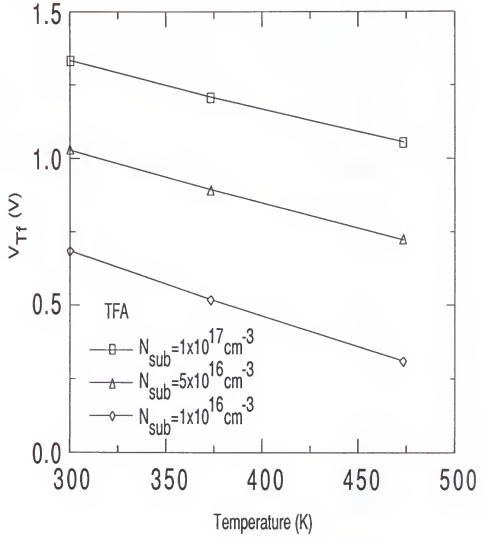


Fig. 3.6 Simulation of variation in threshold voltage of front gate V_{Tf} with temperatures for TFA mode devices (t_b = 0.08μm) having different body doping concentration N_{sub}.

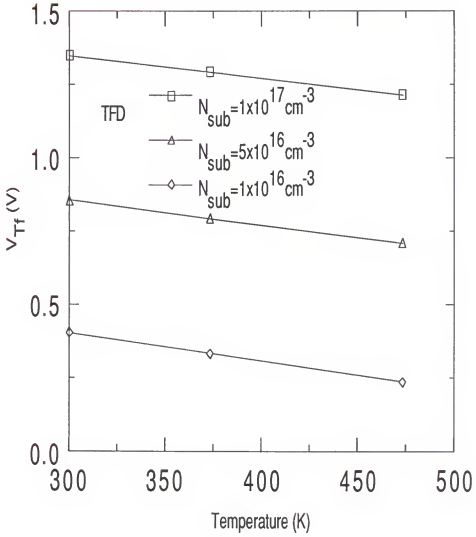


Fig. 3.7 Simulation of variation in threshold voltage of front gate V_{Tf} with temperatures for TFD mode devices (t_b = 0.08μm) having different body doping concentration N_{sub}.

of TFD in Fig. 3.7, as expected. However, the value of V_{Tf} in those figures cannot be directly compared because different values of device parameters have been used for the simulations of devices in Fig. 3.6 and Fig. 3.7. In conclusion, device having larger N_A value has large V_{Tf} and has smaller $|\partial V_{Tf}/\partial T|$ value.

3.3.2 Leakage Current

The measurements of the leakage current due to thermal generation in the reverse-biased body-drain junction are made using the measurement setup in Fig. 3.8 to extract the generation lifetime in the space charge region τ_g in (3.25). In Fig. 3.8, V_D bias of +2 V is applied to drain to make the body-drain junction to become reverse-biased. Body contact is grounded. A large negative bias of -20 V is applied to back gate to suppress leakage current in the back channel by making the back channel accumulated. To separate the effect of thermal generation in the depleted body film from that of thermal generation in the reverse-biased body-drain junction, a bias which is about the same size of the flat-band voltage of the front channel is applied to the front gate in order to prevent the depletion in the body under the front channel. Using the measurement setup in Fig. 3.8, the measurements of the current at each contact has been done and the results are shown in Table 3.1. From Table 3.1, at T=75°C and T=100°C, the current at the drain I_D when V_{GbS} = -20 V is different from that when V_{GbS} =0 V. However I_B doesn't change at either V_{GbS}

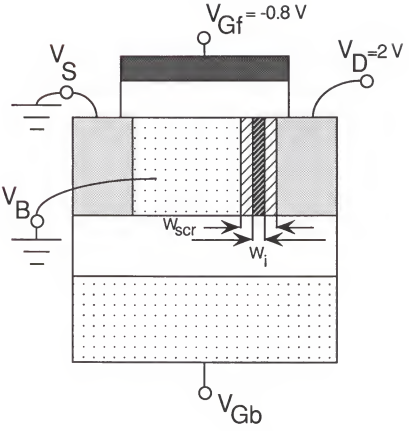


Fig. 3.8 Measurement setup for leakage current which flows through the reverse-biased body-drain junction at several high temperatures.

Table 3.1

Leakage current measured by the setup in Fig. 3.8

Temperature(°C)	V_{GbS} (V)	I_D (pA)	I_B (pA)
75	-20	35.2	-30.1
	0	96.2	-31.8
100	-20	105.6	-105.1
	0	229.5	-107.6
125	-20	296	-283
	0	308	-294
150	-20	771	-779
	0	790	-813
175	-20	3660	-3600
	0	3900	-3570
200	-20	17730	-7420
	0	13890	-7510
50	-20	13.75	-9.15
	0	13.6	-9.4

bias and it is almost equal to I_D when $V_{GbS} = -20$ V. Therefore I_B can be thought as reliable data of the leakage current which flows through the reverse-biased body-drain junction. The dependence of I_D on V_{GB} might be due to the effect of leakage in the back channel. At the range of $125^oC \leq T \leq 175^oC$, $I_D \cong I_B$ at $V_{GbS} = 0$ or -20 V ,which doesn't depend on V_{GB}. This might be due to the fact that the currents through the body-drain junction become large, so the effect of the back channel leakage can be ignored. At $T = 200^oC$, $I_D >> I_B$ and this is because the reduction of the threshold voltage makes the subthreshold current to flow in the channel. At $T = 50^oC$ $I_D > I_B$ regardless of V_{GB} and this might due to the great influence of the leakage current in the back channel in this temperature.

Considering above discussion on the measurements of leakage current, it seems proper to use I_B as $I_{gen,scr}$ in (3.25) for extraction of the generation lifetime in the space charge region τ_g. From (3.25),

$$\tau_g = \frac{q\ n_i\ W_i\ t_b\ Z}{I_{gen,scr}} \tag{3.46}$$

Now the proper range of temperature where (3.25) can be applied must be chosen. The I_B data at $V_{DS} = 2$ V, $V_{BS} = 0$ V, $V_{GfS} = -0.8$ V, $V_{GbS} = -20$ V is plotted in Fig. 3.9 as a function of temperature. In Fig. 3.9, the curves which are proportional to n_i and n_i^2 are also plotted for determination

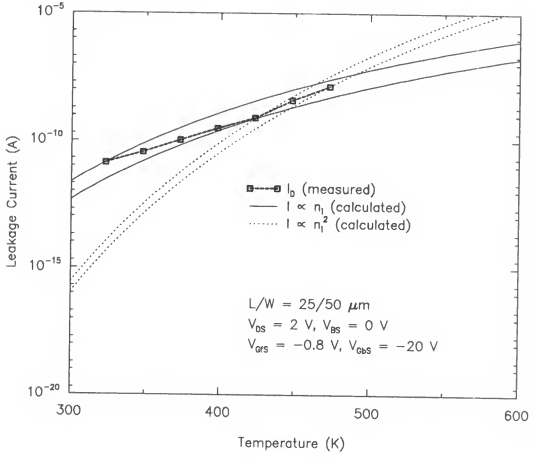


Fig. 3.9 Measured leakage current between reverse-biased body-drain junction in 323 K (50°C) ≤ T ≤ 473 K (200°C). For temperatures above 423 K, the leakage current is predominated by generation in the undepleted body; for temperature below 423 K, it is predominated by generation inside the space charge region of the body-drain junction.

of the range in which the I_B data follows the curve proportional to n_i. As is seen in Fig. 3.9, in the range of $50^oC < T < 150^oC$, I_B data follows the curve proportional to n_i. The fact that I_B follows the curve n_i in this temperature range means that the leakage current is due to the thermal generation inside the space charge region and this is in agreement with the results of Nordquist et al. [Nor89]. According to that [Nor89], below $T = 150^oC$, the generation current inside the space charge region which is proportional n_i is a dominant factor in leakage current through the reverse-biased p-n junction, but, above $T = 150^oC$ the generation current at the edge of neutral region (diffusion current) is dominant. Therefore (3.45) is used in the range of $50^oC < T < 150^oC$ to extract τ_g using I_B as $I_{gen,scr}$. The Levenberg-Marquardt non-linear least square fit is applied to the τ_g value extracted by this way using the τ_g model in (3.39). The results give the parameters of (3.39), $\tau_a = 5.434 \times 10^{-16}$ and $\tau_b = 1.132 \times 10^{-6}$. Comparison between the extracted τ_g and the τ_g calculated by (3.39) is made in Fig. 3.10. Reasonably good fit is obtained. Now, for the simulation of the generation lifetime τ_g, (3.39) having $\tau_a = 5.434 \times 10^{-16}$ and $\tau_b = 1.132 \times 10^{-6}$ will be used. From fits to the leakage current in the subthreshold of SOI MOSFET, $\tau_{no}(300)$ is set to be $\tau_g(300)/1000$ and this value is used in the further simulation of device characteristics.

3.3.3 Channel Mobility

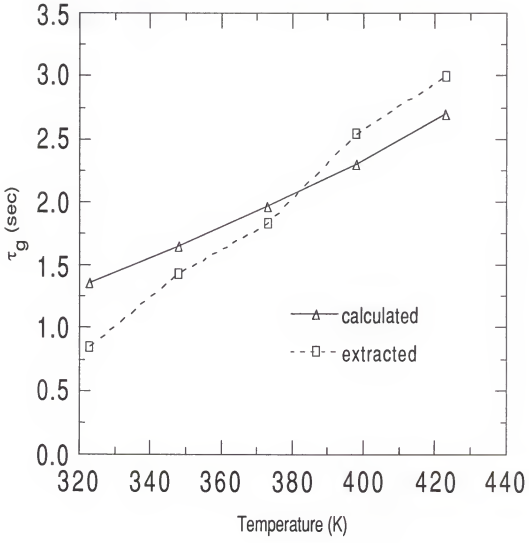


Fig. 3.10 Generation lifetime inside space charge region of body-drain junction, τ_g extracted from measurement of leakage current I_B in Fig. 3.8 and calculated by (3.39).

The channel mobility model in (2.15) of Chapter 2 can be used as the model for channel mobility at high temperature range. Meanwhile, at high temperature, the phonon scattering limited mobility μ_{ph} in (2.11) is a dominant factor in channel mobility, therefore μ_{ph} can represent the whole channel mobility μ_{eff}. Let us compare the results between using (2.15) as μ_{eff} and using μ_{ph} as μ_{eff}. The model parameters for two cases are shown in Table 3.2, which are extracted by Levenberg-Marquardt non linear least square fit. Simulated channel mobility data calculated by the parameters in Table 3.2 are shown in Fig. 3.11 along with the measured data. As is seen in Fig. 3.11, there is little difference in the goodness of fit between two cases, and using μ_{ph} as μ_{eff} is accurate enough. Using μ_{ph} as μ_{eff} has several advantages i.e. there is no need for measurement at high temperature for extraction of mobility parameters and only room temperature measurement is enough and the number of parameter is reduced from five to three. For the further simulation purposes, μ_{ph} is used as μ_{eff}.

Because channel carriers of thin-film SOI MOSFET experience smaller vertical electric field, the channel mobility of the devices is much larger than that at bulk MOSFET or thick-film SOI MOSFET [Stu88, Yos89]. Therefore the drain current of thin-film SOI MOSFET is larger than that of bulk MOSFET or thick-film SOI MOSFET. Comparison of I_D between thin-film(t_b = 0.08 μm) SOI MOSFET and thick-film(t_b=1,2 μm) SOI MOSFET is made and shown in Fig.

Table 3.2

Electron channel mobility model parameters

$\mu_{eff} = \frac{1}{\frac{a_c}{T} + a_p T^n E_{eff}^{1/\gamma} + a_s E_{eff}^2}$	$\mu_{eff} = \mu_{ph} = \frac{1}{a_p T^n E_{eff}^{1/\gamma}}$
$a_c = 8.99 \times 10^{-7}$	
$a_p = 4.67 \times 10^{-8}$	$a_p = 4.42 \times 10^{-8}$
$a_s = 3.91 \times 10^{-18}$	
$n = 1.537$	$n = 1.537$
$\gamma = 6.25$	$\gamma = 6.25$

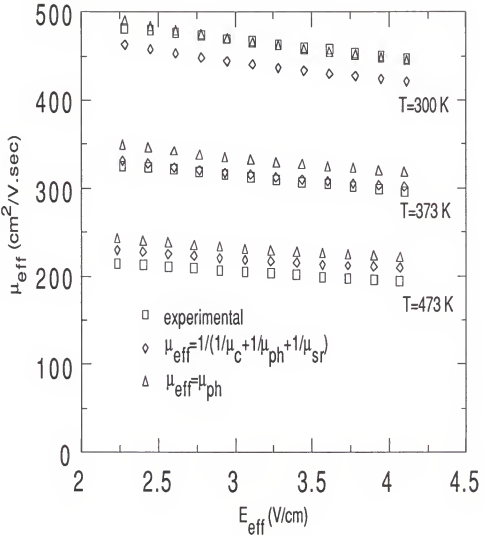


Fig. 3.11 Experimental electron channel mobility extracted from the drain current measurement at small drain bias and calculated electron channel mobility by (2.15) and by (2.11) at T = 300, 373, 473 K.

3.12. There is no proper test devices for thin-film case, so I_D of thin-film case is simulated. It is clear in Fig. 3.12 that I_D of thin-film case is much larger than that of thick-film case, even if the difference of channel mobility is not the only reason for the difference I_D , it made significant difference [Stu88, Yos89]. Due to the difference in magnitude of E_{sf} between TFD and TFA, likewise we can expect larger I_D from TFD. The simulation results in Fig. 3.13 show this trend.

3.3.4 Current due to impact ionization

The generation current due to impact ionization becomes smaller as temperature increases because of (1) the reduction of channel current due to the mobility degradation and (2) reduction of the multiplication factor M due to the decrease of the saturation voltage and the impact ionization rate. The decrease of saturation voltage is caused by the reduction of threshold voltage at high temperature. The reduction of impact ionization rate is due to the increased scattering at high temperature. Measurements of the current through the body contact I_B shows the decrease in current caused by impact ionization. Simulation of I_B is performed and the results show the right trends. At a fixed V_{DS}, but varying V_{GS}, I_B is measured while a negative bias is applied between body and source to insure that body-source junction remains in reverse-biased and I_B flows through body contact. Note here that I_B consists of not only the generation current due

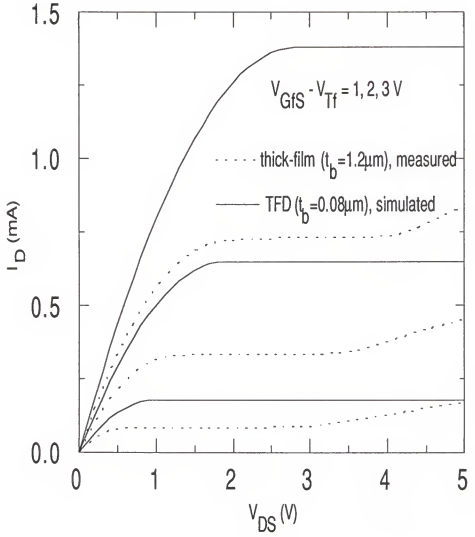


Fig. 3.12 Comparison of I_D of thick-film device (measured) and TFD mode thin-film (simulated) at $V_{GfS} - V_{Tf}$ = 1, 2, 3 V.

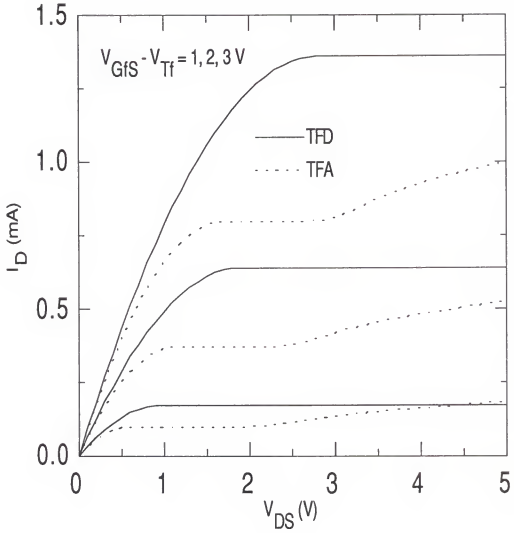


Fig. 3.13 Comparison of simulated I_D of TFD mode and TFA mode of thin-film device at $V_{GfS} - V_{Tf}$ = 1, 2, 3 V.

to impact ionization but also the current due to thermal generation in the depleted body and space charge region at the body-drain junction. In Fig. 3.14, the measured and simulated I_B are shown at T = 27, 100, 200°C. As expected, I_B decreases as temperature increases. However, at T = 200°C, the measured I_B is larger than that at T=27, 100°C. This is due to the increased leakage current by thermal generation. Simulated results do not show this because of the underestimation the leakage current due to thermal generation. The peaks of simulated I_B are shown at larger V_{GfS} value. This is due to the inaccuracy of the simulation of the V_{Tf}. The simulation of device characteristic is done by thin-film SOI MOSFET model [Vee88] where the temperature dependences presented here are implemented. The simulation of thick-film devices using the model can be done by making $t_b = x_{d,max}$ in the TFA mode. This method results in little error in simulation of threshold voltage when $V_{BS} = 0$ V, but when $V_{BS} \neq 0$ V, the error becomes significant.

3.3.5 Current-Voltage Characteristics.

The test devices having $N_{sub} = 10^{17}$ cm^{-3} and $t_b = 0.25$ μm are thick body-film case. The existing thin-film SOI MOSFET model [Vee88] where the temperature-dependent models in this chapter are added can not simulate the test devices because the model is applicable to the thin body-film case. Therefore, simulations for the test devices are made using an alternative method which use TFA case of the thin-film model

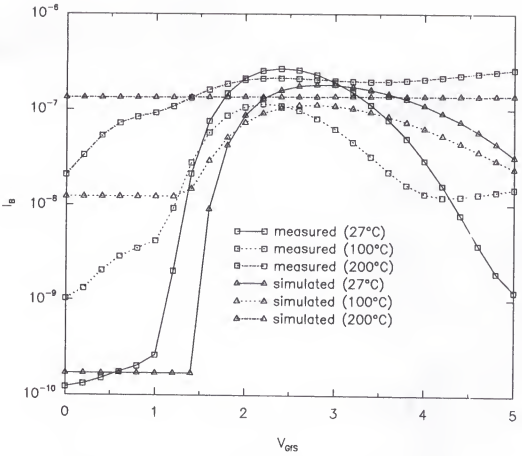


Fig. 3.14 Measured and simulated I_B at T = 27, 100, 200°C.

with t_b set equal to the depletion region width, $x_{d(max)}$, at strong inversion [Fos90].

In Fig. 3.15, measured and simulated I_D-V_{GfS} characteristics at T = 27°C, 100°C, 200°C are shown. From Fig. 3.15, the fitness of the simulated V_{Tf} to the measured V_{Tf} and simulated I_D to the measured I_D is good. In Fig 3.16, Comparison of measured and simulated I_D-V_{GfS} at different temperatures is shown. Here, at small V_{GfS}, I_D at higher temperature is larger because of the reduction of V_{Tf}. However, at large V_{GfS}, I_D at higher temperature is smaller because of the channel mobility degradation. In Fig. 3.17 and 3.18, the measured and simulated I_D-V_{GfS} data in Fig. 3.15 are reformatted on a semilog scale in I_D. It is shown that the subthreshold leakage current increase as temperature increases. The rate of leakage current increase becomes larger at higher temperature. This is due to the fact that the leakage current is proportional to n_i^2 at T > 150°C as seen in section 3.3.2. The fitness of simulated leakage current to the measurement is reasonably good and shows right trends. In Fig. 3.17 and 3.18, the abrupt increase of I_D around $V_{GfS} = V_{Tf}$ and the flat I_D at smaller V_{GfS} are results of incompleteness of subthreshold current model.

The simulated I_D-V_{DS} characteristics of long-channel devices with floating body at T = 27°C, 100°C, and 200°C are shown in Fig. 3.19 along with the measured I_D-V_{DS} data. The fitness of simulation to the measurement in the triode region is reasonably good as already seen in I_D-V_{GfS} characteristics

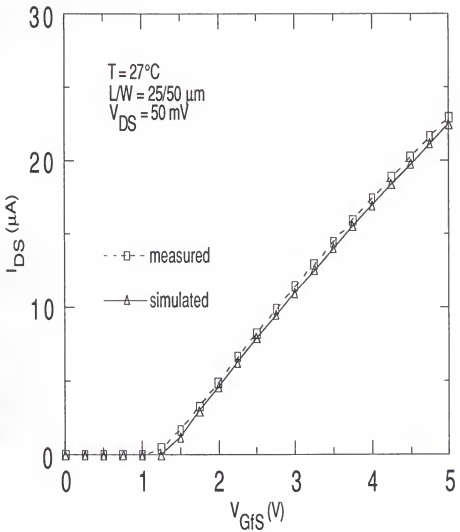


Fig. 3.15 (a) Simulated and measured I_D-V_{GfS} characteristics at T = 27°C.

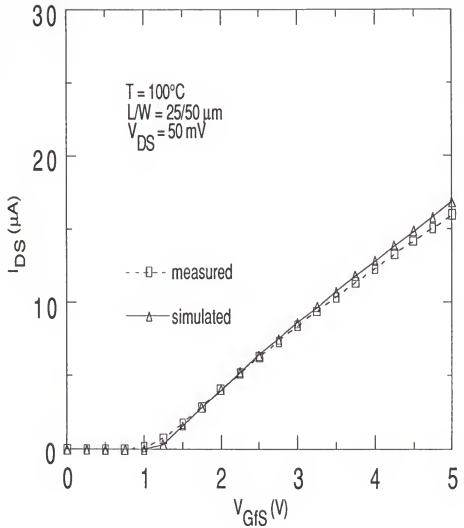


Fig. 3.15 (b) Simulated and measured I_D-V_{Gfs} characteristics at T = 100°C.

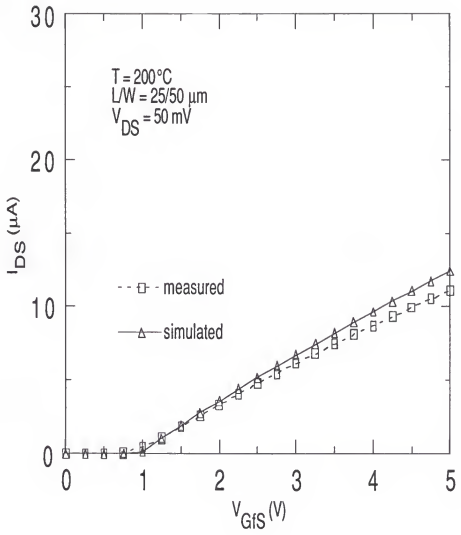


Fig. 3.15 (c) Simulated and measured I_D-V_{GfS} characteristics at T = 200°C.

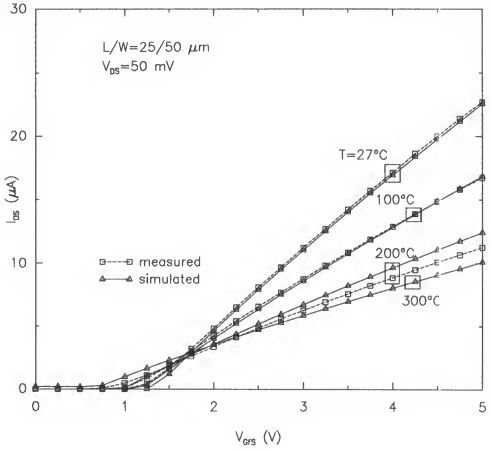


Fig. 3.16 Measured and simulated I_D-V_{GfS} characteristics of a long-channel SOI MOSFET at T = 27, 100, and 200°C. Body contact is floating. For 300°C, simulated characteristic is given.

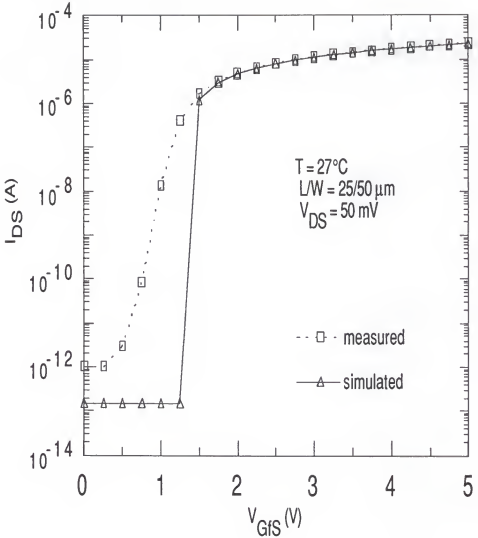


Fig. 3.17 (a) Simulated and measured I_D-V_{GfS} characteristics at T = 27°C. (I_D is in log scale.)

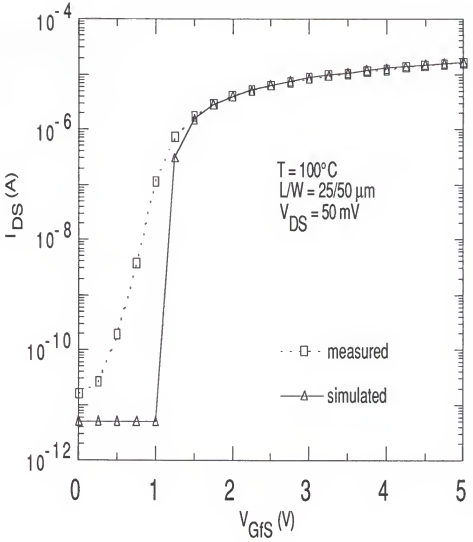


Fig. 3.17(b) Simulated and measured I_D-V_{GfS} characteristics at T = 100°C. (I_D is in log scale.)

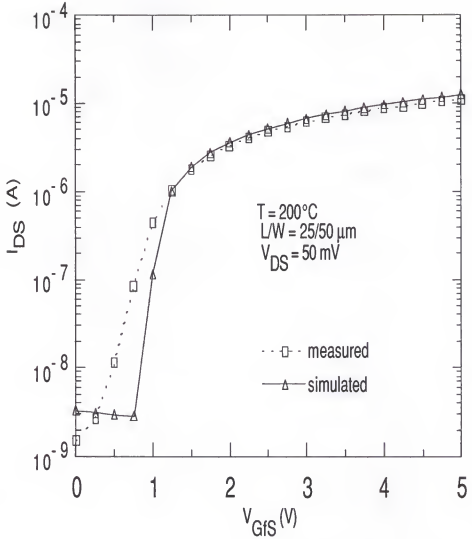


Fig. 3.17 (c) Simulated and measured I_D-V_{GfS} characteristics at T = 200°C. (I_D is in log scale.)

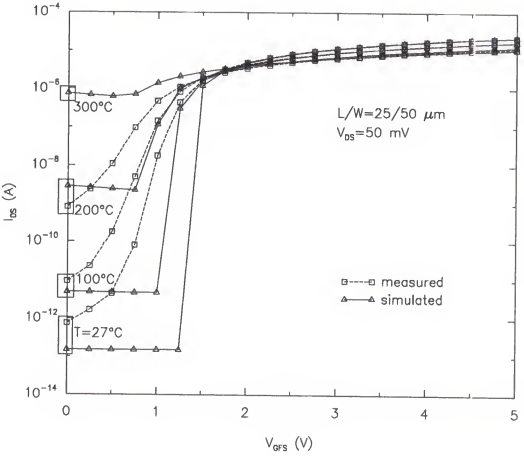


Fig. 3.18 Simulated and measured I_D-V_{GfS} characteristics at T = 27, 100, 200°C when V_{GfS} = 3.5 V. (I_D is in log scale.)

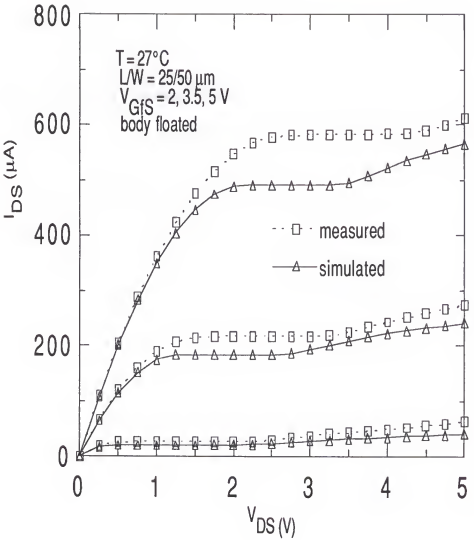


Fig. 3.19 (a) Simulated and measured I_D-V_{DS} characteristics at T = 27°C when V_{GfS} = 2, 3.5, 5V.

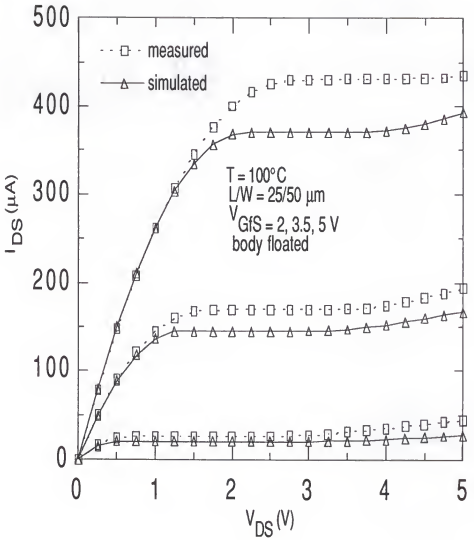


Fig. 3.19 (b) Simulated and measured I_D-V_{DS} characteristics at T = 100°C when V_{GfS} = 2, 3.5, 5V.

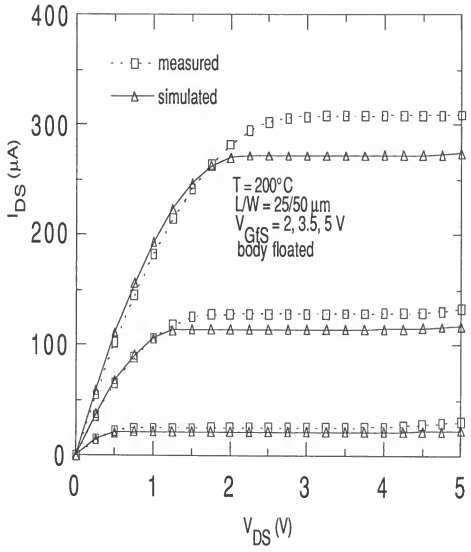


Fig. 3.19 (c) Simulated and measured I_D-V_{DS} characteristics at T = 200°C when V_{GfS} = 2, 3.5, 5V.

simulation in Fig. 3.15, but the simulation method using TFA model with $t_b = x_{d(max)}$ for the thick-film test devices causes some discrepancy in the saturation current level. In the thin-film SOI MOSFET, the saturation current is [Fos90]

$$I_{DS(sat)} \cong \frac{W}{L} \frac{\mu_{eff} C_{of}}{2(1 + C_b/C_{of})} [V_{GfS} - V_{Tf}]^2 \qquad (3.47)$$

The saturation current in the bulk MOSFET is [Bre81]

$$I_{sat} = \frac{W}{L} \mu_{eff} C_{ox} [V_{GS} - V_{T(sat)}]^2 \qquad (3.48)$$

where V_{GfS} and C_{of} in (3.47) is equal to V_G and C_{ox} in (3.48), respectively, and V_{Tf} in (3.47) is equal to $V_{T(sat)}$ in (3.48) when $t_b = x_{d(max)}$. However, m in (3.48) $\neq 1/(2+C_b/C_{of})$ in (3.47), because for the test devices, m $\cong$ 0.33 and $1/(2+C_b/C_{of}) \cong 0.28$. Therefore, the saturation current in (3.48) is about 14 % larger than that in (3.47). In Fig. 3.20, the simulated saturation current given by (3.47) with $t_b = x_{d(max)}$ is about that much smaller than the measured one given by (3.48).

The kink in the I_D-V_{DS} characteristics of SOI MOSFET which has a floating body is caused by the decrease of threshold voltage due to the increase in body potential. The accumulation of holes generated due to impact ionization (in n-channel device) raises the body potential. At higher temperatures, the kink occurs at larger drain bias as seen in

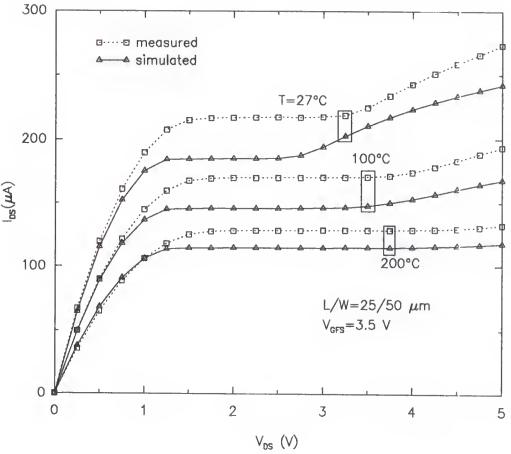


Fig. 3.20 Measured and simulated I_D-V_{DS} characteristics of a long-channel SOI MOSFET at T = 27, 100, 200°C. Body contact is floating. For 300°C, simulated characteristic is given.

Fig. 3.20, because the weak impact ionization decreases with decreasing I_D and (M-1) as can be seen in (3.41). The decrease of (M-1) is due to the increase of $V_{DS(sat)}$ and β_o, the impact ionization parameter. The $V_{DS(sat)}$ slightly increases because the threshold voltage decreases with increasing temperature. The decrease of drain current is due to decrease of channel mobility. The simulated V_{BS} vs V_{DS} at T = 27, 100, 200°C in Fig. 3.21 is seen to show this trend.

3.4 Summary

Several temperature dependent models for device parameters of long-channel SOI MOSFET have been presented. At high temperature, the increase of intrinsic carrier density causes the reduction of the front-channel threshold voltage and the the increase of leakage current in the body-drain junction due to the increased thermal generation in the reverse-biased junction and in the depleted body film. The channel mobility degradation at high temperature due to the increased surface phonon scattering results in reduced drain current. The decrease of drain current and the increase of saturation voltage due to the reduction of threshold voltage cause the reduction of generation by weak impact ionization and hence, the shift in the kink effect to higher drain biases. The models have been implemented in SPICE2. By the physical nature of the models, it has been demonstrated for predictive use in computer-aided device and circuit design.

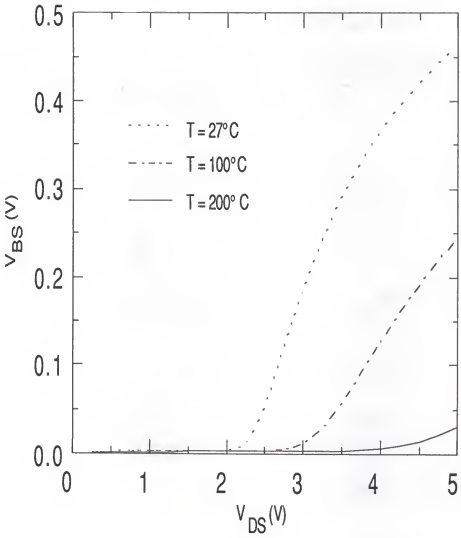


Fig. 3.21 Simulated V_{BS}-V_{DS} characteristics of a long-channel SOI MOSFET at T = 27, 100, 200°C. Body contact is floating.

CHAPTER 4
SIMULATION OF SIMPLE CIRCUITS

4.1 Introduction

The simulation of a high-temperature operation of a CMOS inverter which is a basic building block of CMOS circuitry is performed to demonstrate the functionality of SOI CMOS at high temperature and to show the usefulness of the temperature-dependent SOI MOSFET model proposed in Chapter 3. The model is implemented in SPICE2 [Nag75] for use in circuit simulation. Comparison of the simulated results of circuit performance at room temperature and high temperature (T = 300°C) is made to show the temperature-dependent trends of device characteristics. The simulation of a 5-stage ring oscillator composed of SOI CMOS gates shows that the switching delay at 300°C is about twice that at room temperature.

Another area in which the advantages of SOI technology can be exploited is smart power ICs. There are strong demands for a dielectrically isolated smart-power IC which integrates the power MOSFET with control circuitry on one chip. The reason for this is that the SOI chip is latchup free, has good high-voltage isolation and allows for good circuit design flexibility [Ohn89, Oha87] because of its near perfect isolation. In addition, it has a higher resistance to device degradation because it has a smaller V_{Tf} variation and

this is essential for the smart-power IC operation in a high-temperature environment.

The simulation of a simple smart-power IC consisting of a vertical double-diffused MOS (VDMOS) with SOI CMOS inverters used as the gate drive circuitry is made at T = 27°C and 300°C. For the power VDMOS MOSFET, an existing subcircuit model [Sco90] is used. Each component in this model can be implemented using SPICE2 circuit models. However, for the simulation of high-temperature operation, parameter values at these temperatures are needed. Therefore, the temperature dependences of several parameters of the subcircuit model are investigated. According to the simulation results of this simple smart-power IC, the switching delay at T = 300°C is approximately double that at T = 27°C and the predominant cause for the increased delay is the reduction in current drive capability of the gate drive circuit. The power delivered to the load by the VDMOS is also reduced because of its own reduced drive capability caused by the decrease of the channel mobility at high temperature.

4.2 CMOS inverter and ring oscillator

Simulations of a SOI CMOS inverter and a 5-stage SOI CMOS ring oscillator at several temperature are done to demonstrate the functionality of SOI CMOS at high temperature and to compare the device characteristics between room and high temperature. To facilitate the simulation of CMOS circuitry, the channel mobility of the p-channel SOI MOSFET

is assumed to be approximately half that of n-channel devices. The simulated SOI CMOS inverter consists of TFD mode NMOS and PMOS. The TFD mode devices are chosen because TFD mode devices have better device characteristic at high temperature as pointed in Chapter 3. The simulated voltage transfer characteristics of the inverter at several temperatures are shown in Fig. 4.1. It is seen that at room temperature, the inverter switches state at half the power-supply voltage, because the two devices are almost matched. The NMOS has V_{Tf} of 1 V, $N_{sub} = 10^{17}$ cm^{-3}, W/L = 10 μm/5 μm. The PMOS has V_{Tf} of -1 V, $N_{sub} = 8 \times 10^{16}$ cm^{-3}, W/L = 20 μm/5 μm. Therefore, both have the same magnitude of V_{Tf} and almost the same drain current level as can be seen in Fig. 4.2. However, as temperature increases, the switching tends to occur at larger input voltage. This is caused by the deviation of the device characteristics at high temperature. At high temperature the NMOS and PMOS are no longer matched because of the difference in the threshold voltage as shown in Table 4.1. The threshold voltages of PMOS and NMOS at room temperature are -1 V and 1V, but these are reduced at high temperature and the reduction rates are different because of the difference of body-film doping concentration (see Section 3.3.1). The rate of temperature variation rate in the threshold voltage of PMOS is larger than that of NMOS. This makes the voltage transfer characteristic of the CMOS inverter become asymmetrical as shown in Fig 4.1. At high temperatures the magnitude of the threshold voltage of PMOS

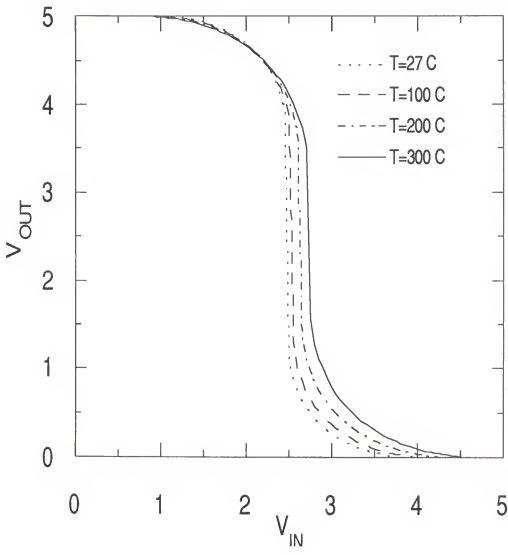


Fig. 4.1 Simulated voltage transfer characteristics of a SOI CMOS inverter at several temperatures. (L/W of NMOS = 5/10 μm and L/W of PMOS = 5/20 μm)

Table 4.1
The simulated values of threshold voltage of NMOS and PMOS at different temperatures.

Temperature (°C)	V_{Tf} of NMOS (V)	V_{Tf} of PMOS (V)
27	1	-1
100	0.945	-0.814
200	0.867	-0.539
300	0.784	-0.249

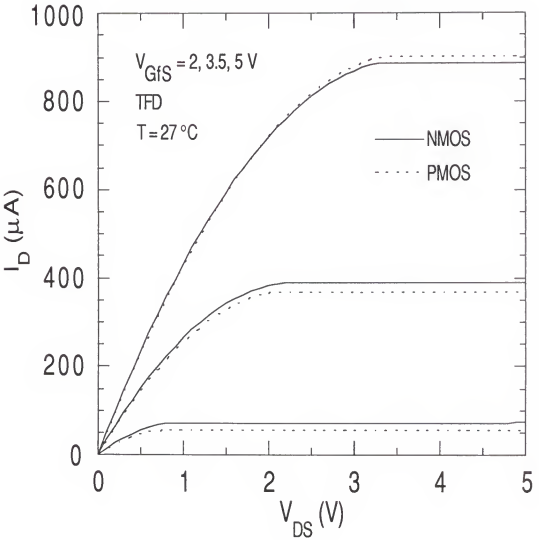


Fig. 4.2 Simulated I_D-V_{DS} characteristics of NMOS and PMOS at T = 27°C which form the SOI CMOS inverter in Fig. 4.1.

is smaller than that of NMOS, so the center of the voltage transfer characteristics in Fig. 4.1 moves right at high temperatures. The smaller threshold voltage of PMOS at high temperature makes the drain current become larger than that of NMOS as shown in Fig. 4.3. As seen in Fig. 4.2, at room temperature the current is almost the same because PMOS and NMOS have matched characteristics. On the other hand, the current of PMOS becomes larger due to the relatively smaller threshold voltage at high temperature. If the matched characteristics between NMOS and PMOS is required for the maximum noise margin of the circuits at high temperature, the fact mentioned above must be carefully considered. The switching response of the SOI CMOS inverter having a capacitor load of same value at T = 27°C and T = 300°C is shown in Fig. 4.4. At T = 300°C, the switching delay is much larger due to the reduced current drive capability caused by the channel mobility degradation as seen in Chapter 3. The switching delay at T = 300°C is about double that at T = 27°C as shown in the simulated results of a 5-stage ring oscillator in Fig. 4.5 and this is in agreement with the experimental observation by Krull et al. [Kru88].

4.3 Smart-Power IC

Simulations for the device and circuit characteristics of smart-power IC which consists of a power VDMOS given in Fig. 4.6 and SOI CMOS inverters for the gate drive circuitry have been performed at T = 27 and 300°C. A subcircuit model is

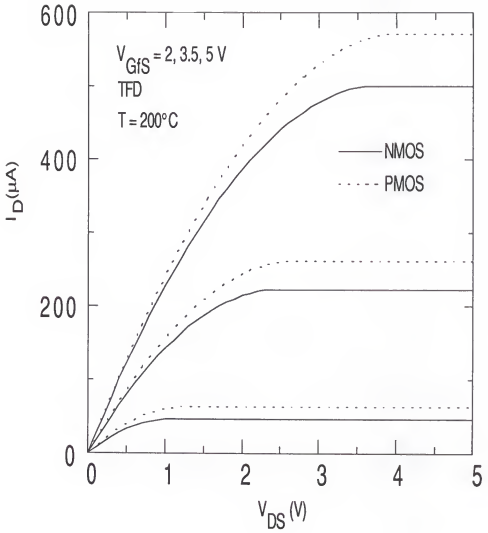


Fig. 4.3 Simulated I_D-V_{DS} characteristics of NMOS and PMOS at T = 200°C which form the SOI CMOS inverter in Fig. 4.1.

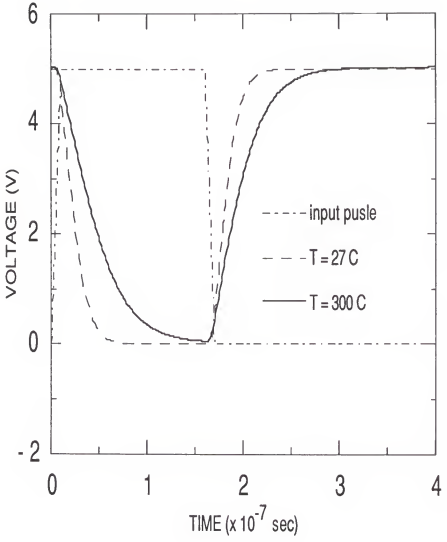


Fig. 4.4 Simulated switching response of a SOI CMOS inverter in Fig. 4.1 at T = 27°C and T = 300°C.

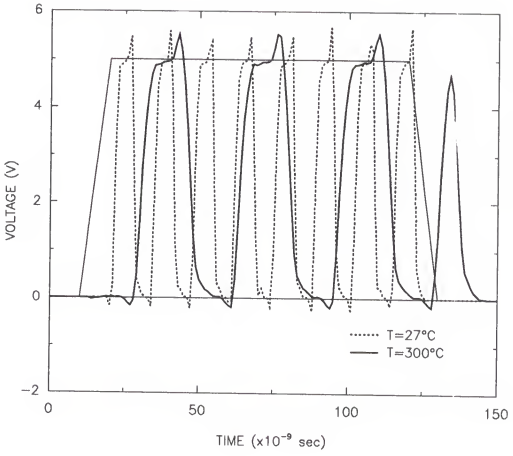


Fig. 4.5 Simulated oscillation of a 5-stage SOI CMOS oscillator at T = 27°C and T = 300°C.

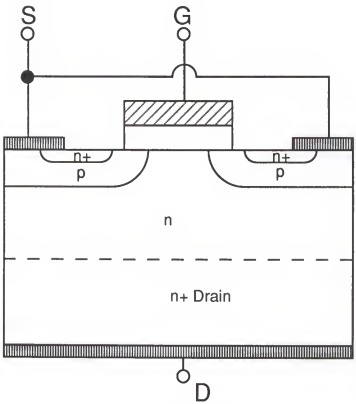


Fig. 4.6 Cross-section of a power VDMOS cell.

chosen for the simulation of power VDMOS, each component of which is represented by SPICE2 models. However, for simulation at T = 300°C, values of temperature-dependent parameters must be determined. The temperature dependence of the channel mobility model parameter, the drain resistance, and the saturation current of parasitic body-drain diode are investigated and the parameter values at high temperature are detemined by following the temperature dependences. Using the parameter values which are determined from their temperature dependences, simulations for the VDMOS DC output characteristics and its reverse recovery response, and the switching responses of smart power switch have been performed. All these results show the right trends.

4.3.1 Temperature Dependences of VDMOS Model Parameters

The subcircuit model in Fig. 4.7 [Sch90] is chosen for the simulation of power VDMOS. Each component of the model can be represented by SPICE2 models for room temperature simulation. In the subcircuit model, two PMOS, M2 and M3 with a voltage source V_{offset}, are used for the simulation of the gate drift region overlap capacitance which is bias-dependent. D_{Sub} is a parasitic diode in the body-drain junction. (The source and the body connections are tied.) The drain resistance is split into R_{d1} and R_{d2} for the best simulation of gate drift region overlap capacitance by M2 and M3. For simulation at T = 300°C, temperature dependences of several device parameters are needed.

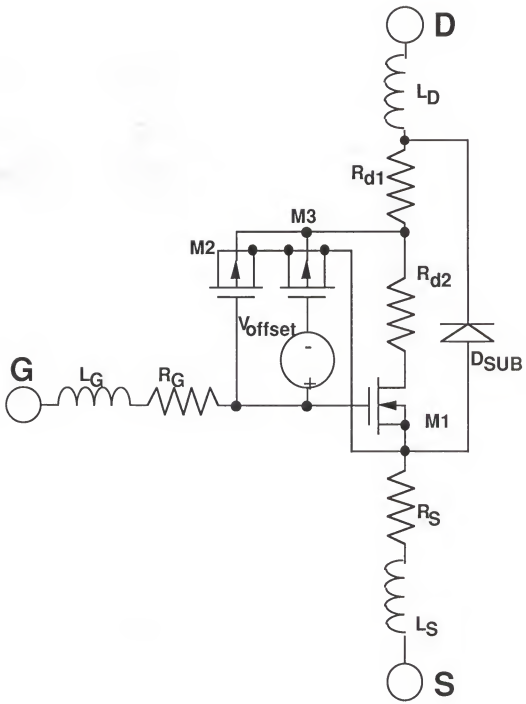


Fig. 4.7 VDMOS subcircuit model.

At high temperatures, surface phonon scattering becomes the dominant scattering mechanism in the channel mobility as seen in Chapter 2. The surface phonon scattering-limited mobility has a temperature dependence proportional to $T^{-1.537}$ as seen in Chapter 3. Using this, the temperature dependence of the SPICE 2 channel mobility parameter μ_o is given

$$\mu_o(T) = \mu_o(300\ K) \left(\frac{T}{300\ K}\right)^{-1.537} . \tag{4.1}$$

The drain resistance R_{d1} and R_{d2} in Fig.4.7 is approximately the sum of the vertical resistance in the bulk epitaxial region and the JFET on-resistance [Sun80a]. According to the literature [Sun80a], both the epitaxial region resistance and the JFET on-resistance are proportional to epitaxial-layer resistivity ρ. Here, epitaxial-layer resistivity ρ is inversely proportional to epitaxial-layer bulk mobility. The epilayer bulk electron mobility has a $T^{-2.42}$ temperature dependence [Jac77]. Therefore,

$$R_d(T) \propto \rho(T) \propto T^{2.42} . \tag{4.2}$$

Using the relation in (4.2),

$$R_{dx}(T) = R_{dx}(300\ K) \left(\frac{T}{300\ K}\right)^{2.42} \tag{4.3}$$

where x = 1 for R_{D1} or = 2 for R_{D2}.

The increase of intrinsic carrier concentration n_i with increasing temperature causes the threshold voltage of the VDMOS to decrease, as seen in the SOI MOSFET in Chapter 3. The temperature-dependent model for n_i in Chapter 3, which has been implemented into SPICE 2, is used.

At the high temperature above 150°C, the diffusion current in the neutral region at the edge of the depletion region in the reverse-biased p/n junction [Sze81] becomes the dominant leakage current. Therefore, for simulation of leakage current in the source-drain diode D_{sub} in Fig. 4.6 the saturation current of SPICE2 diode model is expressed by ideal diode current equation as

$$I_s = Aq\sqrt{\frac{D_p}{\tau_r}}\frac{n_i^2}{N_D} \quad . \tag{4.4}$$

where A is area of the diode, D_p is diffusivity, and τ_r is SRH generation lifetime. The temperature dependences of D_p and τ_r is given as those in chapter 3.

4.3.2 Simulation Results

The simulations of VDMOS characteristics are performed using parameters as seen in Table 4.2. Thick gate oxide (t_{ox} = 100 nm) is chosen in Table 4.2 due to the large gate bias of the power VDMOS, and this causes the threshold voltage to become large. A SOI CMOS inverter used in the gate drive circuit is consisted of NMOS and PMOS which has thin-film

Table 4.2

Model parameters of VDMOS subcircuit in Fig. 4.7

Device	Parameter	when T = 27°C	when T = 300°C
NMOS	L (μm)	2	2
	W (m)	1	1
	AD (μm^2)	20	20
	PD (m)	2	2
	μ_o(cm^2/V.sec)	600	222
	U_{exp}	0.026	0.026
	N_{sub} (cm^{-3})	10^{17}	10^{17}
	N_{ss} (cm^{-2})	2.5×10^{11}	2.5×10^{11}
	C_{GSO} (F)	3.45×10^{-10}	3.45×10^{-10}
PMOS	L (μm)	2.5	2.5
	W (m)	1	1
	N_{sub} (cm^{-3})	10^{15}	10^{15}
D_{SUB}	CJO (F)	27×10^{-10}	30×10^{-10}
	PB (V)	0.98	0.72
	r_{d1} (Ω)	0.05	0.24
	r_{d2} (Ω)	0.05	0.24
	L_S (nH)	7.5	7.5
	L_D (nH)	3.5	3.5
	T_{ox} (nm)	100	100

(thickness = 500 Å) body, 25nm-thick gate oxide. The NMOS has L = 5μm and W = 11μm, and PMOS has L = 5μm and W = 20μm.

The simulated VDMOS DC output characteristics at T = 27°C and 300°C are shown in Fig. 4.8. At T = 300°C, the drain saturation voltages are significantly greater than those at T = 27°C due to the reduction of threshold voltage V_{th}. In fact, V_{th} at T = 300°C is 1.765 V while it is 3.535 V at T = 27°C. The degradation of channel mobility at T = 300°C causes the decrease in the drain current level. Interestingly, at V_{GS} = 5 V, the current level at T = 300°C is higher than the counterpart at T = 27°C. This is due to the reduction of V_{th} at T = 300°C.

The simple smart power IC to be simulated is shown in Fig. 4.9 with a resistor load and ten SOI CMOS inverters as the gate drive circuit. The simulated turn-on and turn-off switching responses of the circuit at T = 27°C and 300°C are shown in Fig. 4.10 and 4.11. The simulated switching waveforms at several nodes have typical shapes as can be seen in the textbook, for example, [Gra89]. In the turn-on transients, there is no change in V_{DS} until V_{GS} reaches V_{th}. Once V_{GS} becomes equal to V_{th}, V_{DS} starts to decrease down to $V_{DS(ON)}$ and I_{DS} starts to increase to $I_{DS(ON)}$. However, V_{GS} changes little because most of the gate current flows through the gate-drain overlap capacitance which is magnified by the Miller effect. After V_{DS} settles down to $V_{DS(ON)}$, V_{GS} begins to increase again. A larger switching delay occurs at T = 300°C. This is due to the reduced current drive capability of SOI

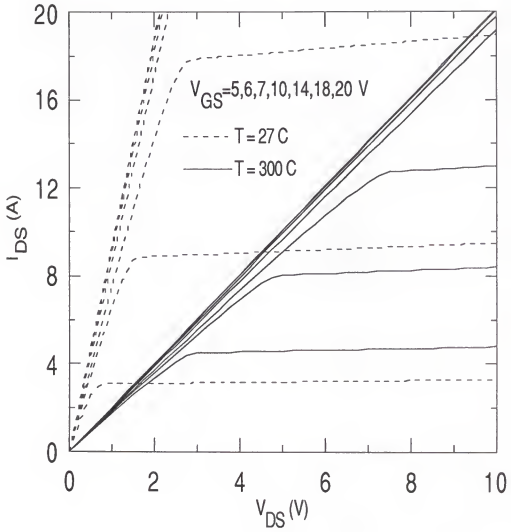


Fig. 4.8 I_D vs V_{DS} characteristic of a VDMOS simulated by SPICE 2 using the subcircuit model in Fig. 4.7 with parameters in Table 4.2 at T = 27°C and T = 300°C.

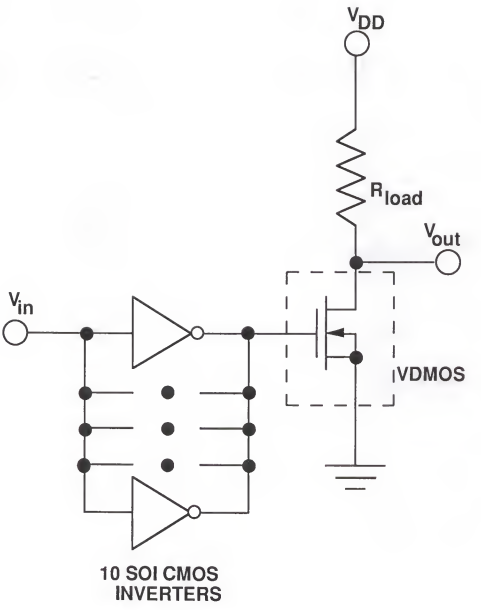


Fig. 4.9 A transient response test circuit of a VDMOS power switch with a resistive load and 10 SOI CMOS inverters as a gate drive circuit. R_{load} is 3.7 Ω at T = 27°C and is 17.7 Ω at T = 300°C.

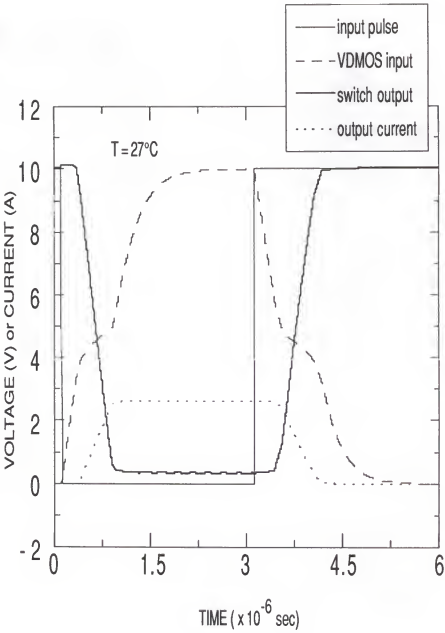


Fig. 4.10 Simulated transient response of the smart power switch in Fig. 4.9 at T = 27°C.

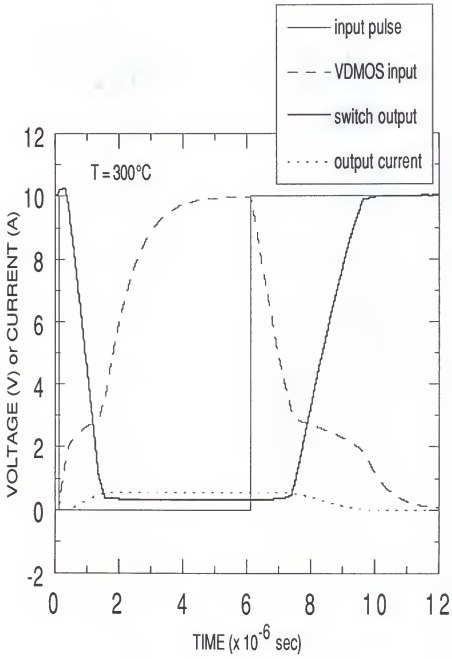


Fig. 4.11 Simulated transient response of the smart power switch in Fig. 4.9 at T = 300°C.

CMOS inverters at T = 300°C caused by the degradation of channel mobility. The current level which can be delivered to the load by the power switch in the on-state is reduced at T = 300°C. (See Fig. 4.10 and 4.11.)

Reverse recovery problems of the parasitic source-drain diode D_{sub} may arise when using power MOSFETs in multiple transistor configurations. The simulated reverse recovery response of the source-drain diode of VDMOS at T = 27°C and 300°C is shown in Fig. 4.12. A slightly better response is obtained at T = 300°C because of the reduced drain current.

4.4 Summary

Simulation of a SOI CMOS inverter has been performed and demonstrates that SOI CMOS inverter functions well at 300°C. However, the switching delay of the inverter at 300°C is about twice that at room temperature as shown in the simulated ring oscillator operation. This is due to the reduced current drive capability caused by the channel mobility degradation at 300°C. Unequal reduction in threshold voltage of PMOS and NMOS at high temperature due to the difference in body-film doping concentration causes the voltage transfer characteristic of CMOS inverter to become asymmetrical, even if it is symmetrical at room temperature. This unequal reduction in threshold voltage causes the current level of NMOS and PMOS to become somewhat different at high temperatures, although they are almost identical at room temperature. For the maximum noise margin of the circuits at

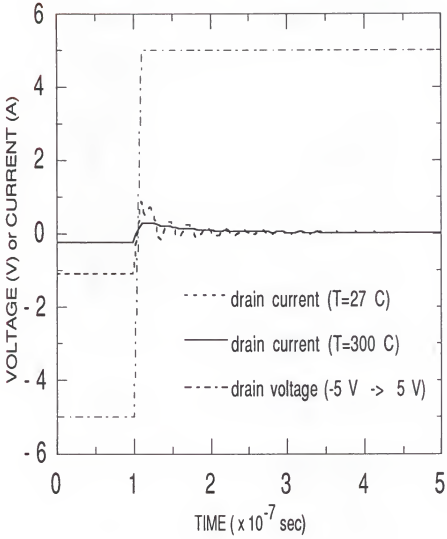


Fig. 4.12 Simulated reverse recovery response of the source-drain diode of VDMOS at T = 27°C and 300°C.

high temperature, these fact must be carefully considered in circuit design.

A simple smart power integrated circuit has been simulated at T = 27°C and T = 300°C. The logic and control circuit consists of the SOI CMOS inverters which drive the gate of a VDMOS power switch. For the simulation of VDMOS, an existing subcircuit model is used. However, for simulations at T = 300°C, the temperature dependences of several parameters of the subcircuit model has been investigated. From SPICE 2 simulations, it is shown that the smart power circuit is functional at T = 300°C, however, the switching delay of the circuit at 300°C is double that at 27°C because of the reduced current drive capability of the SOI CMOS inverters. The power delivered to the load by the VDMOS has also decreased, but the reverse recovery characteristic of the parasitic body-drain diode is comparable.

CHAPTER 5
CONCLUSION AND SUGGESTIONS FOR FUTURE WORK

In this dissertation, a new model for the temperature dependence of the SOI MOSFET for high applications has been developed which, in a physical approach, accounts for the reduction in threshold voltage, the increase of leakage current, channel mobility degradation, and the reduction in the kink effect in the I_D-V_{DS} characteristics. A physically based channel mobility model which covers a wide temperature range (77K-573K) is also developed which considers the effect of three dominant scattering mechanisms in the carrier transport in the MOSFET channel. These models are implemented in SPICE2. Through simulations of devices and circuits and comparisons with measurements, the models have been demonstrated to be useful tools for device and circuit design. Simulation for high temperature operation of a smart power IC which uses SOI CMOS inverters as gate drive circuit has been successfully performed. The smart power IC is another area in which the advantages of SOI technology can be exploited.

There are several points where further investigations can be quested. In Chapter 2, only electron channel mobility is developed. For the accurate simulation of CMOS circuitry, the development of temperature-dependent channel mobility for hole can be targeted for future work.

In Chapter 3, recombination lifetime is determined by direct comparison between the simulated I_D-V_{GfS} and measured I_D-V_{GfS} in semilog scale. Instead of this method, the direct determination of recombination lifetime can be pursued through measurements.

Due to lack of subthreshold model, the accurate simulation of leakage current and subthreshold slope can't be accomplished. Development of a subthreshold model is highly recommended for the accurate estimation of leakage current.

The simulation of smart power IC is attempted in Chapter 4. The use of SOI MOSFET in the smart power IC is a new application area for SOI technology. The smart power IC which is used at high temperatures needs a circuit simulation tool. Therefore, the temperature-dependent model for a power MOSFET needs to be developed for the circuit and device design.

In addition, the physical nature of the models can be utilized to improve existing device structures.

APPENDIX A
DERIVATION OF $W_i(y)$

The rate of thermal generation of electron-hole pairs by SRH theory in the space charge region of reverse biased p-n junction is spacially constant and at its maximum in the region W_i where p and n << n_i and drops to negligible values outside of the region as soon as the condition p and n << n_i is not fulfilled [Cal72]. The region W_i is usually considerably smaller than W_{scr} because in W_{scr}, p and n << $|N_D - N_A|$ and $|N_D - N_A|$ is greater than n_i by several orders. According to Calzolari et al. [Cal72], W_i for strongly asymmetrical p-n junction like the source-body or body-drain junction of NMOS is

$$W_i = \sqrt{\frac{2\ \varepsilon_s\ kT}{q^2\ N_A}} \left[\sqrt{\ln\left(\frac{N_A}{n_i}\right) - \frac{q\ V}{kT}} - \sqrt{\ln\left(\frac{N_A}{n_i}\right)}\right] \qquad (A.1)$$

where V is the applied reverse bias. We are going to find a region like W_i in the depletion region under the front gate oxide of the thin-film SOI MOSFET and of the thick-film SOI MOSFET which is also applicable for bulk MOSFET.

$W_i(y)$ for the depletion region of thick-film SOI or bulk MOSFET

Using depletion approximation in Poisson's equation, we can find an expression for potential in the depletion region, $\phi(x)$, [Bre81]

$$\phi(x) = \phi_s\left(1 - \frac{x}{x_d}\right)^2, \qquad 0 < x < x_d \tag{A.2}$$

where $\phi(x_d)$ is assumed to be zero. At a point x in the depletion region (see Fig. A.1)

$$n(x) = n_i \exp\left(\frac{E_{fn} - E_i(x)}{kT}\right) \tag{A.3}$$

$$p(x) = n_i \exp\left(\frac{E_i(x) - E_{fp}}{kT}\right) \tag{A.4}$$

where it is assumed that E_{fn} and E_{fp} are flat, that is, are not functions of x. By (A.3) if $E_i(x) > E_{fn}$ then $n(x) << n_i$, and by (A.4) if $E_{fp} > E_i(x)$, then $p(x) << n_i$. From Fig. A.1, when $\phi(x) = \phi_B$, then $E_{fp} = E_i(x)$ and when $\phi(x) = \phi_B + V_y(y)$, then $E_{fn} = E_i(x)$. Therefore, in the range of x where $\phi_B \leq \phi(x) \leq \phi_B + V_y(y)$, $p(x)$ and $n(x) << n_i$. By rearranging (A.2) for x, and defining $W_i(y)$

$$W_i(y) = x_2(y) - x_1(y)$$

$$= x_d(y)\left(1 - \sqrt{\frac{\phi_B}{\phi_s}}\right) - x_d(y)\left(1 - \sqrt{\frac{\phi_B + V_y(y)}{\phi_s}}\right)$$

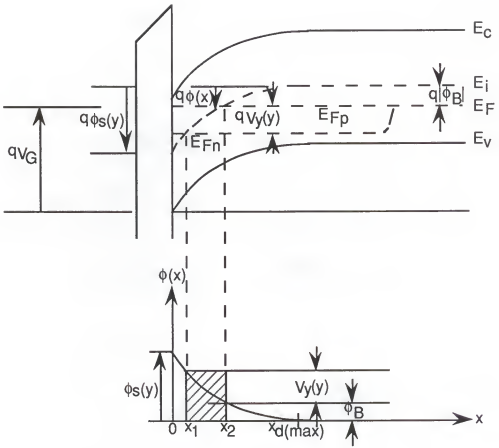


Fig. A.1 Diagrams for energy band and electric potential in a thick-film n-channel MOSFET at a point y along the channel. The x-direction is the direction from the surface into the body film.

$$= x_d(y) \frac{\sqrt{\phi_B + V_y(y)} - \sqrt{\phi_B}}{\sqrt{\phi_s}} \qquad (A.5)$$

where $x_2(y)$ is a point in the depletion region where $\phi(x_2) = \phi_B$ and $x_1(y)$ is a point in the depletion region where $\phi(x_1) = \phi_B + V_y(y)$. At the drain end of the channel where $V_y(L) = -V_{BD}$,

$$W_i(L) = x_d \frac{\sqrt{\phi_B - V_{BD}} - \sqrt{\phi_B}}{\sqrt{\phi_s}} \qquad (A.6)$$

Likewise at the source end of the channel where $V_y(0) = -V_{BS}$,

$$W_i(0) = x_d \frac{\sqrt{\phi_B - V_{BS}} - \sqrt{\phi_B}}{\sqrt{\phi_s}} \qquad (A.7)$$

When $V_{BS} \leq 0$, then $W_i(0) \geq 0$. When $V_{BS} > 0$, $W_i(y) = 0$ where $V_y(y) = \phi_B$. However, the point y where $V_y(y) = \phi_B$ and $W_i(y) = 0$ is not easily found because $V_y(y)$ is a complicated function of y, so we assume $W_i(0) = 0$, for simplicity.

$W_i(y)$ for thin-film SOI MOSFET

Integration of Poisson's equation across the fully depleted body film yields the following expression for the potential in the film body [Lim83]

$$\phi(x) = \psi_{sf} - E_{sf} x + \frac{qN_A}{2\varepsilon_s} x^2 \qquad (A.8)$$

where E_{sf} is given by (3.13). By rearranging (A.9) for x,

$$\frac{qN_A}{2\,\varepsilon_S}\,x^2 \;-E_{sf}\,x + \psi_{sf} - \phi(x) = 0 \qquad (A.9)$$

and solving the above quadratic equation,

$$x = \frac{E_{sf} - \sqrt{E_{sf}^2 - \dfrac{2\,qN_A}{\varepsilon_S}\left(\psi_{sf} - \phi(x)\right)}}{\dfrac{qN_A}{\varepsilon_S}},\quad 0 \le x \le t_b \qquad . \qquad (A.10)$$

Then, using the definition of $W_1(y)$ in (A.6) (see Fig. A.2),

$$W_1(y) = x_2(y) - x_1(y)$$

$$= \frac{E_{sf} - \sqrt{E_{sf}^2 - \dfrac{2qN_A}{\varepsilon_S}\left(\psi_{sf} - \phi_B\right)}}{\dfrac{qN_A}{\varepsilon_S}}$$

$$- \frac{E_{sf} - \sqrt{E_{sf}^2 - \dfrac{2qN_A}{\varepsilon_S}\left(\psi_{sf} - \phi_B - V_y(y)\right)}}{\dfrac{qN_A}{\varepsilon_S}}$$

$$= \frac{\varepsilon_S}{qN_A}\left[\sqrt{E_{sf}^2 - \frac{2qN_A}{\varepsilon_S}\left(\psi_{sf} - \phi_B - V_y(y)\right)} - \sqrt{E_{sf}^2 - \frac{2qN_A}{\varepsilon_S}\left(\psi_{sf} - \phi_B\right)}\right]$$

. (A.11)

At the drain end of the channel where $V_y(L) = -V_{BD}$.,

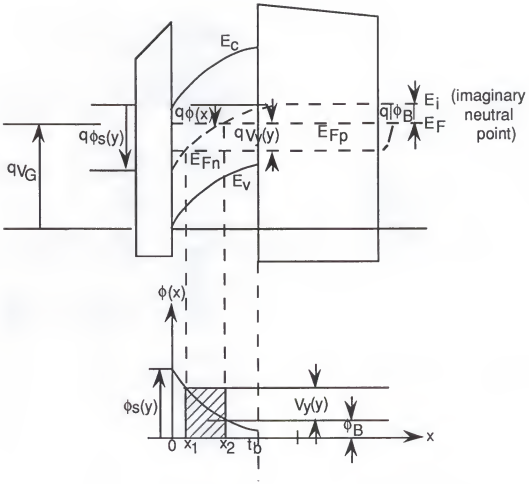


Fig. A.2 Diagrams for energy band and electric potential in a thin-film n-channel SOI MOSFET at a point y along the channel. The x-direction is the direction from the surface into the body film.

$$W_i(L) = \frac{\varepsilon_S}{qN_A}\left[\sqrt{E_{sf}^2 - \frac{2qN_A}{\varepsilon_S}\left(\psi_{sf} - \phi_B - V_{BD}\right)} - \sqrt{E_{sf}^2 - \frac{2qN_A}{\varepsilon_S}\left(\psi_{sf} - \phi_B\right)}\right]$$

. (A.12)

And at the source end of the channel where $V_y(0) = -V_{BS}$,

$$W_i(0) = \frac{\varepsilon_S}{qN_A}\left[\sqrt{E_{sf}^2 - \frac{2qN_A}{\varepsilon_S}\left(\psi_{sf} - \phi_B - V_{BS}\right)} - \sqrt{E_{sf}^2 - \frac{2qN_A}{\varepsilon_S}\left(\psi_{sf} - \phi_B\right)}\right]$$

. (A.13)

When $V_{BS} \leq 0$, $W_i(0) \geq 0$, when $V_{BS} > 0$, we assume $W_i(0) = 0$ using the same reasoning as in the end of previous Section.

APPENDIX B
IMPLEMENTATION OF CHANNEL MOBILITY MODEL INTO SPICE2

The models presented in Chapter 2 and 3 except for channel mobility model are straightforwardly implemented into SPICE2 by replacing the existing models or parameters. Channel mobility model cannot be directly implemented into SPICE2. Channel mobility model is used in the derivation of drain current equation in the existing thin-film SOI MOSFET model of room temperature operation [Vee88]. In the existing model [Vee88], the channel current in the triode region is given

$$I_{DS} = \frac{W \bar{\mu}_{eff} \left(Q^2_{cf}(0) - Q^2_{cf}(L)\right)}{2 C_{of} (1 + \alpha) L \left(1 + \frac{\bar{\mu}_{eff}}{2 v_{sat}} V_{DS}\right)} \qquad (B.1)$$

where $Q_{cf}(0)$, $Q_{cf}(L)$ is inversion layer carrier at source end or drain end, and $\bar{\mu}_{eff}$ is spatially independent mobility model and is defined [Vee88],

$$\bar{\mu}_{eff} \equiv \frac{\mu}{1 - f_B B V_{DS}} \qquad (B.2)$$

where μ, ϕ_B, B are parameters for mobility model used in the existing model. $\bar{\mu}_{eff}$ in (B.2) is intended to be used at a specific temperature. Therefore, the temperature-dependent

channel mobility model presented in chapter 2 should replace $\bar{\mu}_{eff}$ in (B.2) for temperature dependent operation. $\bar{\mu}_{eff}$ is an average of channel mobility along the channel, so it should be replaced by average of channel mobility which is determined by the temperature-dependent model. The average of channel mobility is given by

$$\langle \mu_{eff} \rangle = \frac{\sum Q_{cf}(y)\ \mu_{eff}(y)}{\sum Q_{cf}(y)} \qquad (B.3)$$

where $Q_{cf}(y)$ is inversion layer carrier at a point y along the channel and $\mu_{eff}(y)$ is a channel mobility in a point y along the channel which is determined by the temperature-dependent model. Now $\langle \mu_{eff} \rangle$ in (B.3) replaces $\bar{\mu}_{eff}$ in (B.1). Note μ in (B.2) is $\bar{\mu}_{eff}$ when $V_{DS} = 0$. Therefore it can be replaced by μ_{eff} at source end.

REFERENCES

[And77] T. Ando, "Screening effect and quantum transport in a silicon inversion layer in strong magnetic fields," J. Phys. Soc. Japan, vol. 43, pp. 1616-1626, 1977.

[And82] T. Ando, A. B. Fowler and F. Stern, " Electronic properties of two-dimensional systems," Rev. Mod. Phys., vol. 54, pp. 437-672, 1982.

[Aro87] N. D. Arora and G. SH. Gildenblat, "A semi-empirical model of the MOSFET inversion layer mobility for low-temperature operation," IEEE Trans. Electron Devices, vol. ED-34, pp. 89-93, 1987.

[Bar71] H. D. Barber, "Effective mass and intrinsic carrier concentration in silicon," Solid State Elec., vol. 10, pp. 1039-1051, 1971

[Bla74] W. Blaudau, A. Onton, and W. Heinke, "Temperature dependence of the bandgap of silicon," J. Appl. Phys., vol. 45, pp. 1846-1974, 1974.

[Bre81] J. R. Brews, *Physics of the MOS Transistor*, D. Kahng., Ed., *Silicon Integrated Circuits, Part A*, Academic Press, New York, 1981.

[Bro87] R. B. Brown, F. L. Terry, and K.-C. Wu, "High temperature microelectronics - Expanding the applications for smart sensors," IEDM Tech. Dig., 1987, pp. 274-277.

[Cal72] P. C. Calzolari and S. Graffi, "A theoretical investigation of the generation current in Si p-n junctions under reverse bias," Solid State Elec., vol. 15, pp. 1003-1011, 1972.

[Cha80] K. M. Cham and R. G. Wheeler, "Temperature-dependent resistivities in silicon inversion layers at low temperatures," Phys. Rev. Lett., vol. 44, pp. 1472-1475, 1980.

[Cul90] G. W. Cullen and M. T. Duffy, "Silicon-on-insulator (SOI) applications: Will history be repeated?," Proc. of 4th international Symp.on SOI Technology and Devices, pp. 10-18, 1990.

[Dra79] B. L. Draper and D. W. Palmer, "Extension of high-temperature electronics," IEEE Trans. Components, Hybrids Manufact. Technol., vol. CHMT-2, pp. 399-404, 1979.

[Eza74] H. Ezawa, S. Kawaji, and K. Nakamura, "Surfons and the electron mobility in silicon inversion layers," Japan. J. Appl. Phy., vol. 13, pp. 126-155, 1974.

[Fer79] D. K. Ferry, " The transport of electrons in quantized inversion and accumulation layers in III-V compounds," Thin Solid Films, vol. 56,pp. 243-252, 1979.

[Fos81] J. G. Fossum, M. A. Shibib, "An analytic model for minority-carrier transport in heavily doped region of silicon devices, " IEEE Trans.Electron Devices, vol. ED-28, pp. 1018-1025, 1981.

[Fos90] J. G. Fossum, J. Y. Choi, and R. Sundaresan, "SOI Design for competitive CMOS VLSI," IEEE Trans. Electron Devices, vol. ED-37, pp. 724-729, 1990.

[Gae77] F. H. Gaensslen, V. L. Rideout, E. J. Walker, and J. J. Walker, " Verysmall MOSFET's for low-temperature operation," IEEE Trans. Electron Devices, vol. ED-24, pp. 218-229, 1977.

[Gil85] G. Gildenblat, L. Colonna-Romano, D. Lau, and D. E. Nelson, "Investigation of cryogenic CMOS performance," IEDM Tech. Dig., pp. 268-271, 1985.

[Gra89] D. A. Grant and J. Gowar, *POWER MOSFETs Theory and Applications*, New York: Wiley, 1989.

[Han86] S. Hanamura, M. Aoki, T. Masuhara, O. Minato, Y. Sakai, and T. Hayashida, "Operation of bulk CMOS devices at very low temperatures," IEEE J. Solid-State Circuits, vol. SC-21, pp. 484-490, 1986.

[Har80] A. Hartstein, A. B. Fowler and M. Albert, "Temperature dependence of scattering in the inversion layer," Surface Sci., vol. 98, pp. 181-190, 1980.

[Hart76] A. Hartstein, T. H. Ning and A. B. Fowler, "Electron scattering in silicon inversion layers by oxide and surface roughness," Surface Sci., vol. 58, pp. 181-190, 1976.

[Hew86] HP 94445a TECAP system user's manual, Hewlett-Packard Company , 1986.

[Hos85] B. J. Hosticka, K-.G. Dalsaβ, D. Krey, and G. Zimmer, "Behavior of analog MOS integrated circuits at high temperature, " IEEE J. Solid-State Circuits, vol. SC-20, pp. 871-874, 1985.

[Jac77] C. Jacoboni, C. Canali, G. Ottaviani, and A. A. Quaranta, "A review of some charge transport properties of silicon, " Solid-State Electron., vol. 20, pp. 77-89, 1977.

[Kaw69] S. Kawaji, "The two-dimensional lattice scattering mobility in a semiconductor inversion layer," J. Phys. Soc. Japan, vol. 27, pp. 906-908, 1969.

[Kaw80] Y. Kawaguchi, T. Suzuki and S. Kawaji, "Carrier concentration dependence of mobility in Si (100) n-channel inversion layers at low temperatures," Solid State Comm., vol. 36, pp. 257-259, 1980.

[Kru88] W. A. Krull and J. C. Lee, "Demonstration of the benefits of SOI for high temperature operation," Proc. of 1988 IEEE SOS/SOI Technology Workshop, ST. Simons Island, Georgia.

[Lau84] S. E. Laux, "Accuracy of an effective channel length/external resistance extraction algorithm for MOSFET's," IEEE Trans. Electron Devices, vol. ED-31, pp. 1245-1251, 1984.

[Lim83] H. K. Lim and J. G. Fossum, "Threshold voltage of thin-film SOI MOSFET's," IEEE TRANS. Electron Devices, vol. ED-30, pp. 1244-1251, 1983.

[Lim85] H. K. Lim and J. G. Fossum, "A charge-based large-signal model for thin-film SOI MOSFET's," IEEE Trans. Electron Devices, vol. ED-32, pp.446-457, 1985.

[Lin88] M. S. Lin, "A better understanding of the channel mobility of Si MOSFET's based on the physics of quantized subbands," IEEE Trans. Electron Devices, vol. ED-35, pp. 2406-2411, 1988.

[Lom88] C. Lombardi, S. Manzini, A. Saporito, and M. Vanzi, "A physically based mobility model for numerical simulation of nonplanar devices," IEEE Trans. Computer-Aided Design, vol. CAD-7, pp. 1164-1170, 1988.

[Nag75] L. W. Nagel, "SPICE2: A computer program to simulate semiconductor circuits," Electron. Res. Lab, Univ. of California, Berkeley, ERL Memo, ERL-M520, May 1975.

[Mat74] Y. Matsumoto and Y. Uemura, "Scattering mechanism and low temperature mobility of MOS inversion layers," Japan. J. Appl. Phys., suppl. 2,pt. 2, pp. 367-370, 1974.

[Mor79] S. Mori and T. Ando, "Intersubband scattering effect on the mobility of a Si (100) inversion layer at low temperatures," Phys. Rev. B, vol. 19, pp. 6433-6441, 1979.

[Nie82] W. C. Nieberding and J. A. Powell, "High-temperature electronic requirements in aeropropulsion systems," IEEE Trans. Industrial Electronics, vol. IE-29, pp. 103-106, 1982.

[Nor89] S. E. Nordquist, J. W. Haslett, F. N. Troffimenkoff, "High-temperature leakage current suppression in CMOS ICs, " Electronics Lett., vol. 25, pp. 1133-1135, 1989.

[Oha87] Y. Ohata and T. Izumita, "Dielectrically isolated intelligent power switch, " presented at IEEE 1987 Custom Integrated Circuits Conference, pp. 443-446.

[Ohn89] T. Ohno, S. Matsumoto, and K. Izumi, "Development of key components for SIMOX intelligent power LSIs, " Electronics Lett., vol. 25, pp. 1071-1072, 1989.

[Pre86] W. H. Press, B. P. Flannery, S. A. Teukolsky, and W. T. Vetterling, NUMERICAL RECIPES: The Art of Scientific Computing, Cambrigde, Cambridge University Press, 1986, ch. 14.

[Sab79] A. G. Sabnis and J. T. Clemens, " Characterization of the electron mobility in the inverted <100> Si surface," 1979 IEDM Tech. Dig., pp. 18-21.

[Sah72] C. T. Sah, T. H. Ning and L. L. Tschopp, " The scattering of electrons by surface oxide charges and by lattice vibrations at the Si-SiO2 interface," Surface Sci., vol. 32, pp. 561-575, 1972.

[Sch82] D. K. Schroder, "The concept of generation and recombination lifetime in semiconductors," IEEE Trans. Electron Devices, vol. ED-29, pp. 1336-1338, 1982.

[Sch84] D. K. Schroder, J. D. Whitefielf, and C. J. Varker, "Recombination lifetime using the pulsed MOS capacitor," IEEE Trans. Electron Devices, vol. ED-31, pp.462-466, 1984.

[Sco90] R.S. Scott and G. A. Franz, "An accurate model for power DMOSFETs including interelectrode capacitances,

" Proceedings of IEEE Power Specialist Conf., pp. 113-119, June 1990.

[Sel89] S. Selberherr, "MOS device modeling at 77 K," IEEE Trans. Electron Devices, vol. ED-36, pp. 1464-1474, 1989.

[Sho76] W. Shockley, Electrons and Holes in Semiconductors, Robert E. Krieger Publishing Co., New York, 1976.

[Ste72] F. Stern, "Self-consistent results for n-type Si inversion layer," Phys. Rev. B., vol. 5, pp. 4891-4899, 1972.

[Ste78] F. Stern, "Two-subband screening and transport in (001) Si inversion layers," Surface Sci., vol. 73, pp. 197-206, 1978.

[Ste80] F. Stern, "Calculated temperature dependence of mobility in Si inversion layers," Phys. Rev. Lett., vol.44, pp. 1469-1472, 1980.

[Stu88] J. C. Sturm, "Performance advantages of submicron silicon-on-insulator devices for ULSI, " Proc. Mat. Res. Soc. Symp., vol. 107, pp. 295-307, 1988.

[Sun80a] S. C. Sun and J. D. Plummer, "Modeling of the on-resistance of LDMOS, VDMOS, and VMOS power transistors, " IEEE Trans. Electron Devices, vol. ED-27, pp. 356-376, 1980.

[Sun80b] S. C. Sun and J. D. Plummer, "Electron mobility in inversion and accumulation layers on thermally oxidized silicon surfaces," IEEE Trans. Electron Devices, vol. ED-27, pp. 1497-1508, 1980.

[Sze81] S. M. Sze, Physics of Semiconductor Devices, 2nd Ed., John Wiley & Sons, 1981.

[Tsi82] Y. Tsividis, "Moderate inversion in MOS devices," Solid State Electron., vol. 25, pp. 1099-1104, 1982.

[Tya83] M. S. Tyagi and R. Van Overstraeten, "Minority carrier recombination in heavily-doped Si," Solid State Elec., vol.26, pp. 577-597, 1983.

[Vee88] S. Veeraraghavan and J, G. Fossum, "A physical short-channel model for the thin-film SOI MOSFET applicable to device and circuit CAD," IEEE Trans. Electron Devices, vol. ED-35, pp. 1866-1875, 1988.

[Yos88] M. Yoshimi, H. Hazama, M. Takahashi, S. Kanybayashi, H. Tango, "Observation of mobility enhancement in

ultrathin SOI MOSFETs, " Electron. Lett., vol. 24, pp. 1078-1079, 1988.

[Yos89] M. Yoshimi, H. Hazama, M. Takahashi, S. Kanybayashi, T. Wada, K. Kato, and H. Tango, "Two-dimensional simulation and measurement of high-performance MOSFET's made on a very thin SOI film, " IEEE Trans. Electron Devices, vol. ED-36, pp. 493-503, 1989.

BIOGRAPHICAL SKETCH

Deok-Su Jeon was born in KyungNam, Korea, in 1956. He received the B. S. degree in engineering from the Seoul National University, Seoul, Korea, in 1978, and the M. S. degree in electrical engineering in 1985 from the University of Florida, Gainesville, where he is currently enrolled as a Ph. D. student.

He worked as a research engineer in Hong-Loong Machinery Corporation from 1978 to 1983, where he was engaged in the development of control systems.

His research interests are modeling, simulation and characterization of silicon devices and circuits.

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Dorothea E. Burk, Chairman
Professor of Electrical Engineering

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Jerry G. Fossum
Professor of Electrical Engineering

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Sheng S. Li
Professor of Electrical Engineering

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Robert M. Fox
Assistant Professor of Electrical Engineering

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Kevin S. Jones
Assistant Professor of Materials Science and Engineering

This dissertation was submitted to the Graduate Faculty of the College of Engineering and to the Graduate School and was accepted as partial fulfillment of the requirements for the degree of Doctor of Philosophy

December, 1990

for Herbert A. Beers
Winfred M. Phillips
Dean, College of Engineering

Madelyn M. Lockhart
Dean, Graduate School